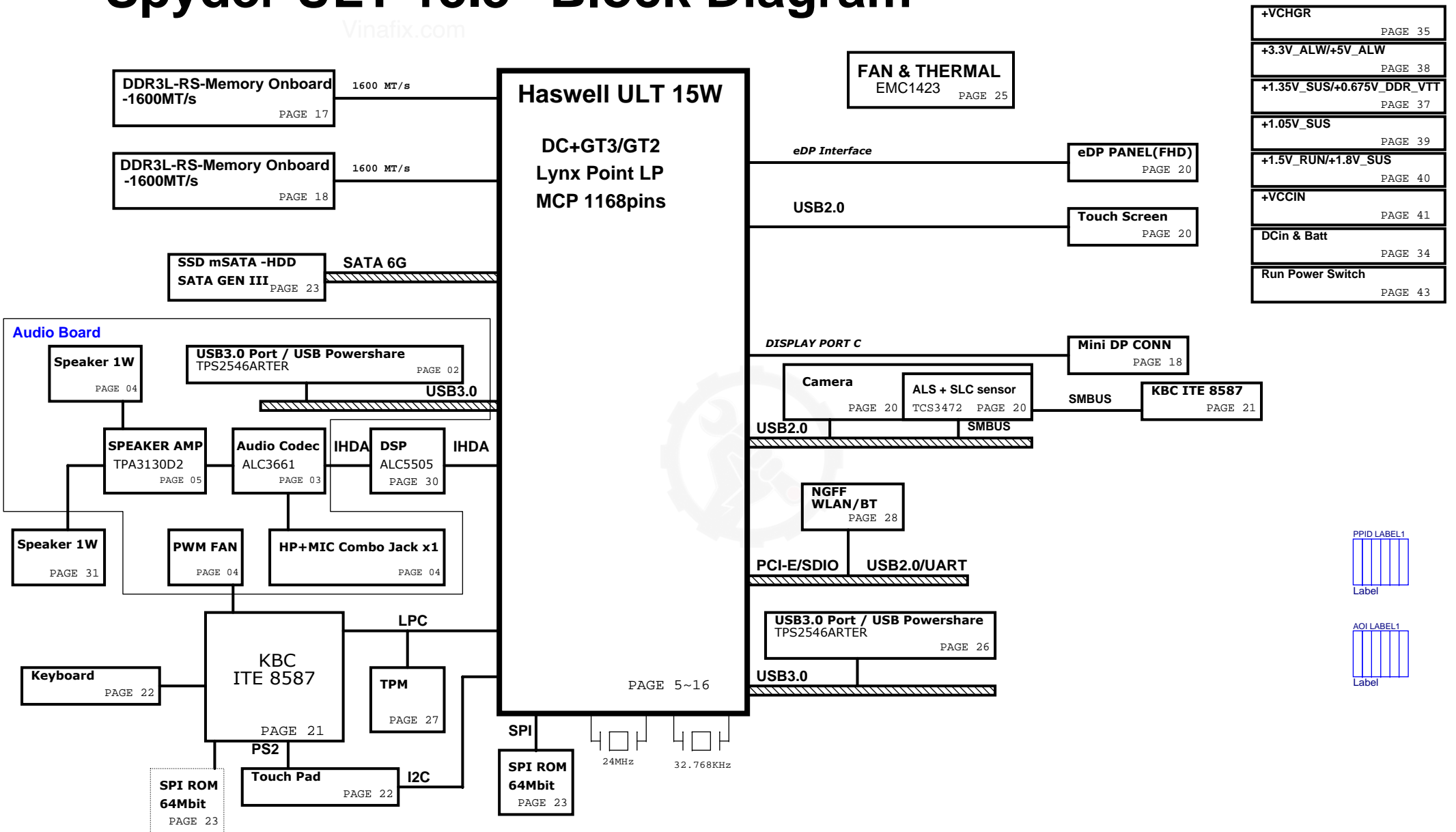


Spyder ULT 13.3" Block Diagram

Vinafix.com



Power State	SLP_S3#	SLP_S4# SLP_S5#	+3.3V_DSW	+15V_ALW	+5V_ALW +3V_ALW	+3.3V_DEEP_SLEEP_OFF	+VDDQ_VR	+0.675V_DDR_VTT	+5V_RUN +3.3V_RUN +1.5V_RUN	+1.05V_RUN	+VCCIN	+V1.05S_VCCST
S0	H	H	H	H	H	H	H	H	H	H	H	H
S3	L	H	H	H	H	H	L	L	L	L	L	L
S4/S5 AC	L	L	H	H	H	L	L	L	L	L	L	L
S4/S5 DC Only	L	L	H	L	L	L	L	L	L	L	L	L
AC/DC Not Exist	L	L	L	L	L	L	L	L	L	L	L	L
Deep Sx	L	L	H	H	L	L	L	L	L	L	L	L
CS AC	L	L	H	H	H	L	L	L	L	L	L	L
CS DC Only	L	L	H	L	L	L	L	L	L	L	L	L

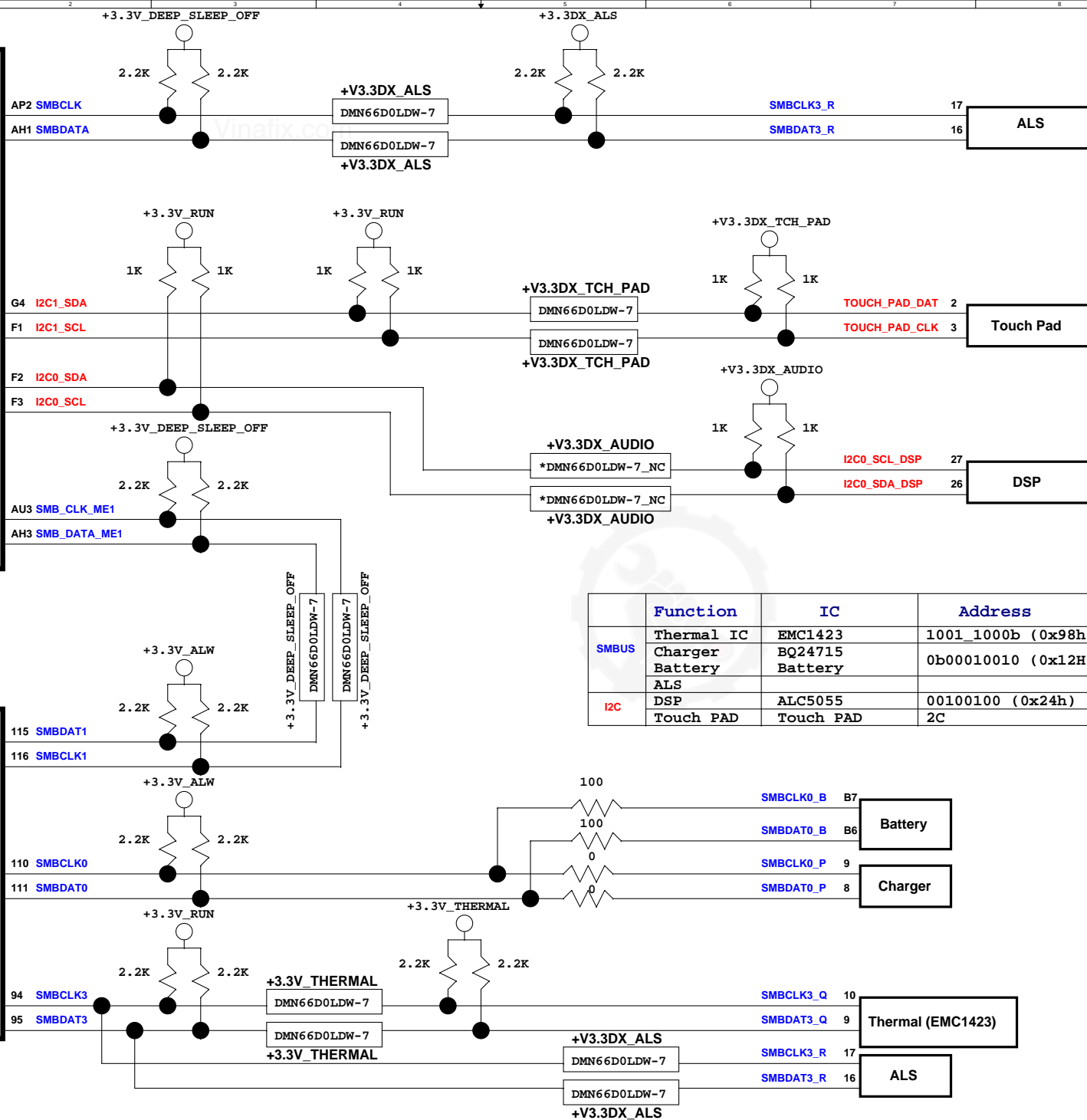


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PROJECT : D13C

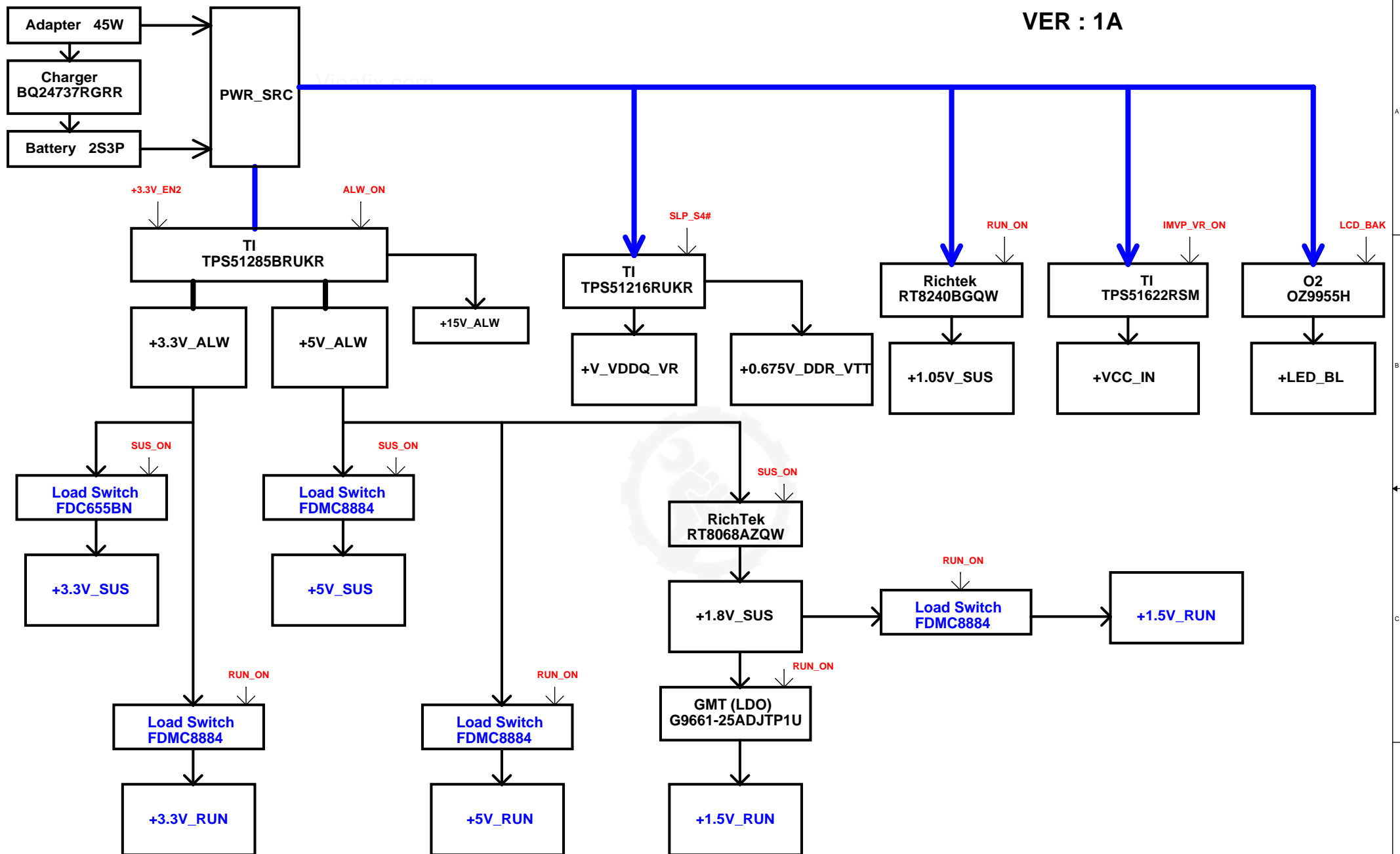
Haswell
ULT

SIO
ITE8587



	Function	IC	Address
SMBUS	Thermal IC	EMC1423	1001_1000b (0x98h)
	Charger	BQ24715	0b00010010 (0x12H)
	Battery	Battery	
	ALS		
I2C	DSP	ALC5055	00100100 (0x24h)
	Touch PAD	Touch PAD	2C

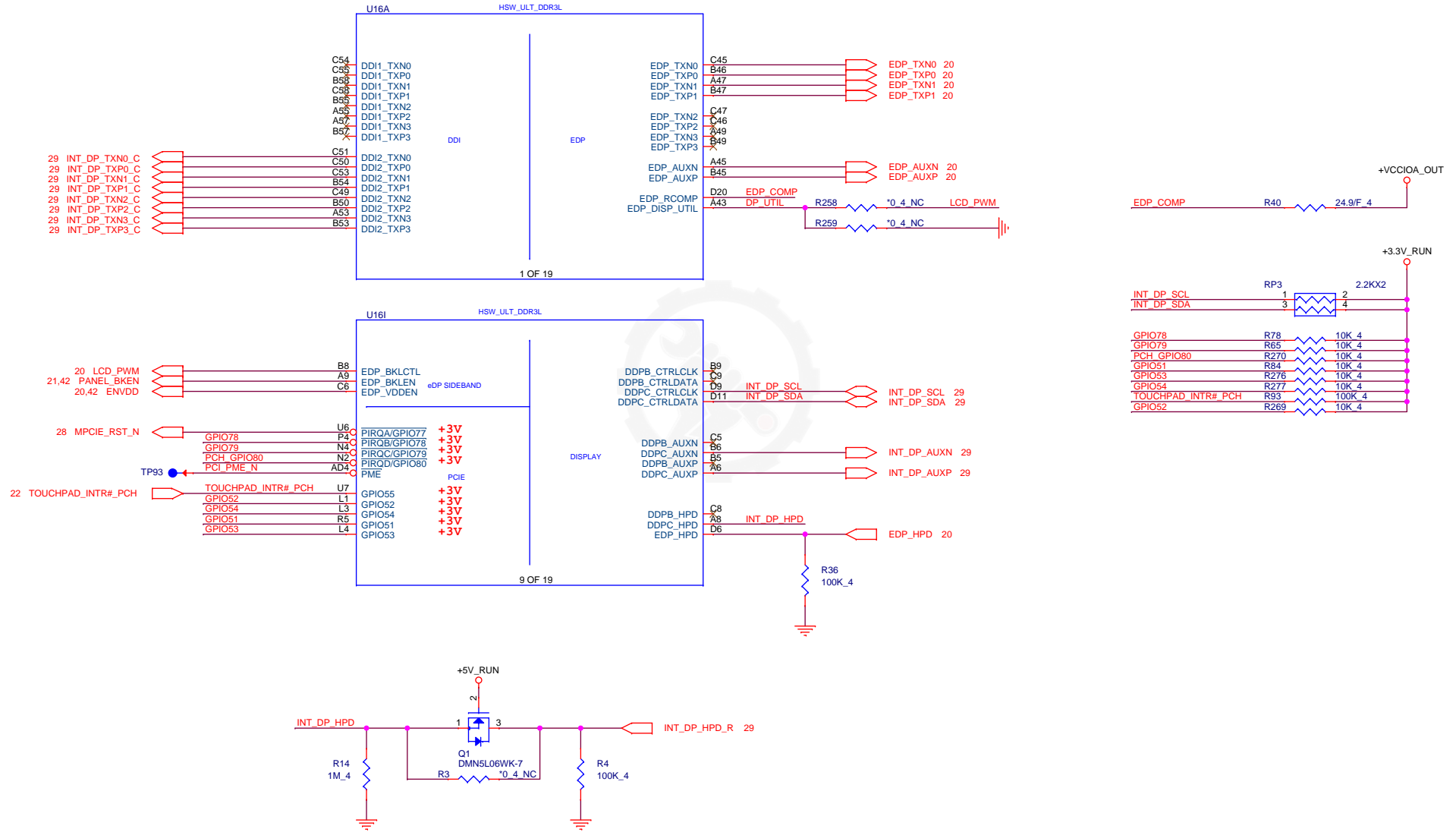
VER : 1A



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Haswell ULT (Display/eDP)



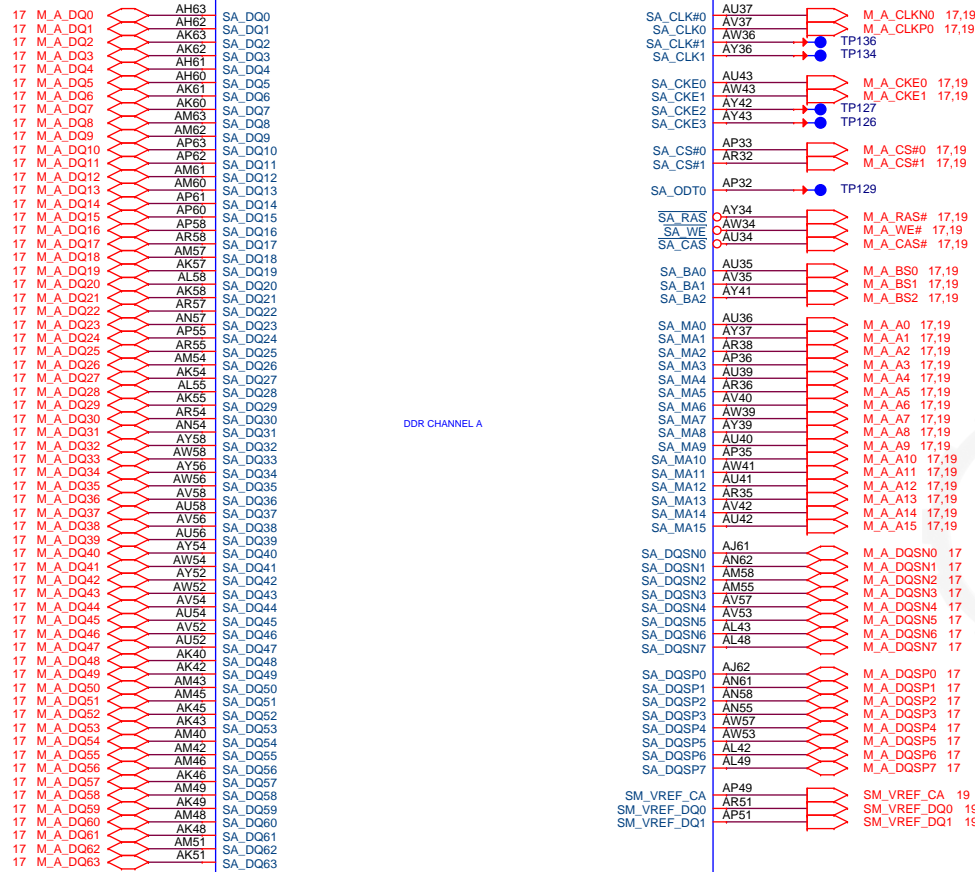
Quanta Computer Inc.

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Haswell ULT (DDR3L-RS)

Vinafix.com

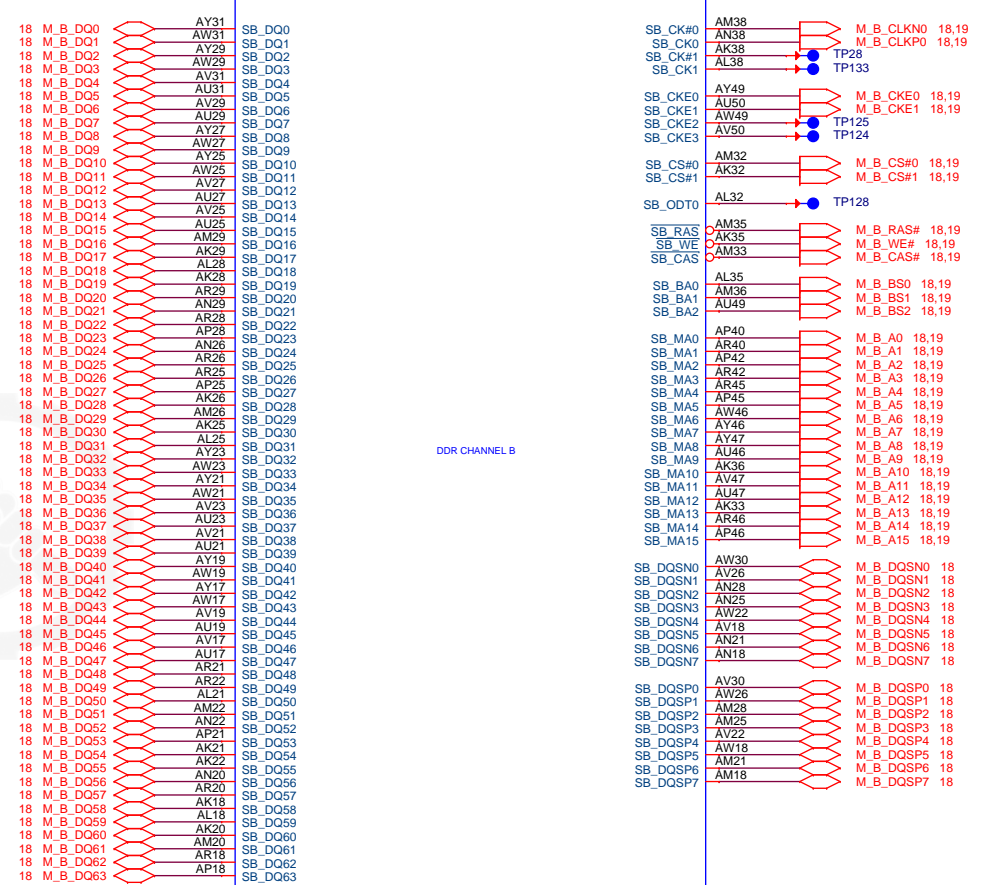
U16C HSW_ULT_DDR3L



DDR CHANNEL A

3 OF 19

U16D HSW_ULT_DDR3L



DDR CHANNEL B

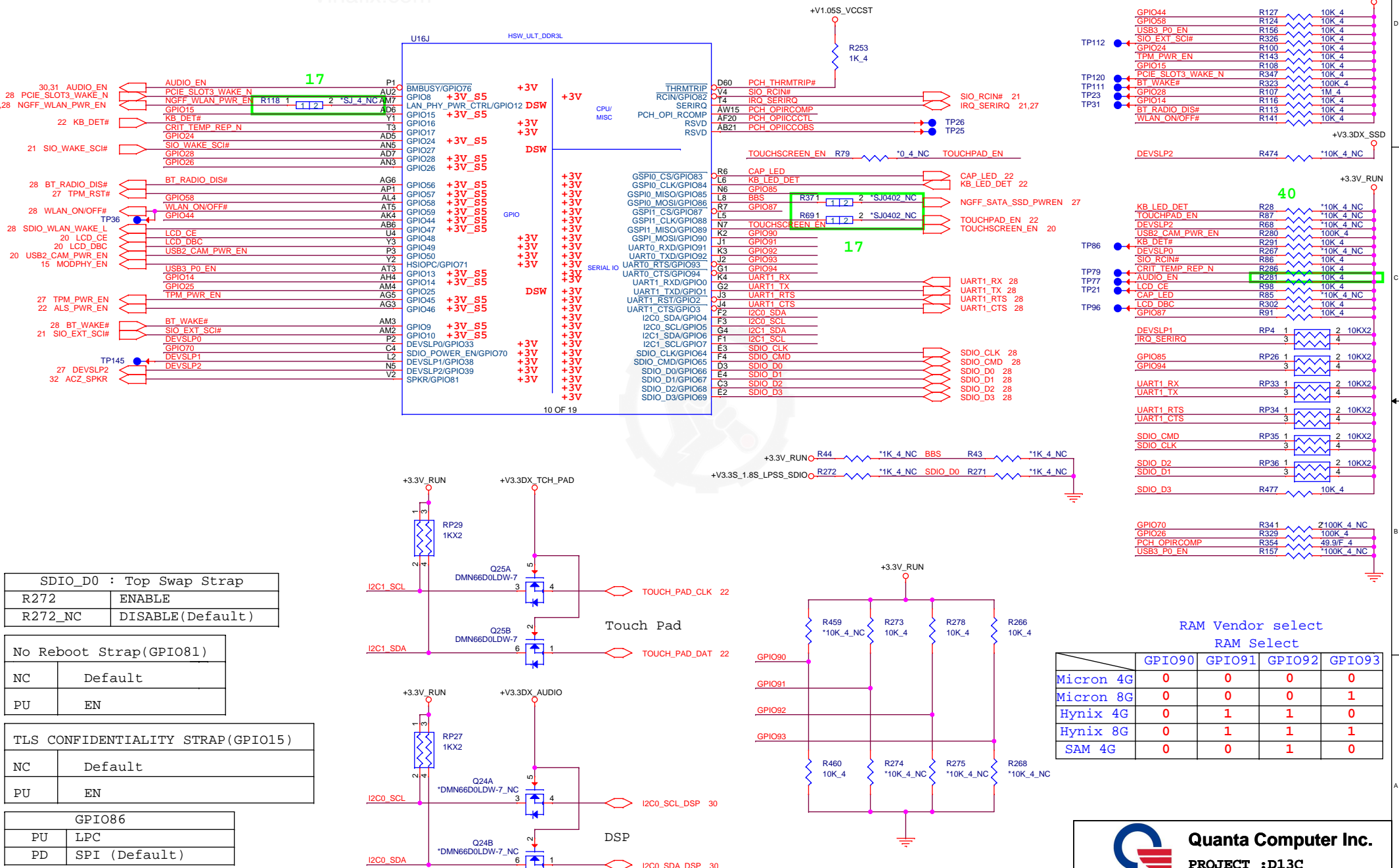
4 OF 19



Quanta Computer Inc.
PROJECT :D13C

Hasswell ULT (GPIO,LPIO,MISC)

GPIO Pull-up/Pull-down (CLG)



SDIO_D0 : Top Swap Strap	
R272	ENABLE
R272_NC	DISABLE(Default)

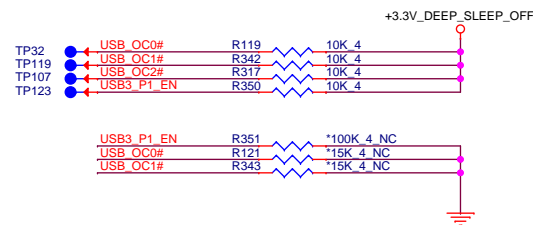
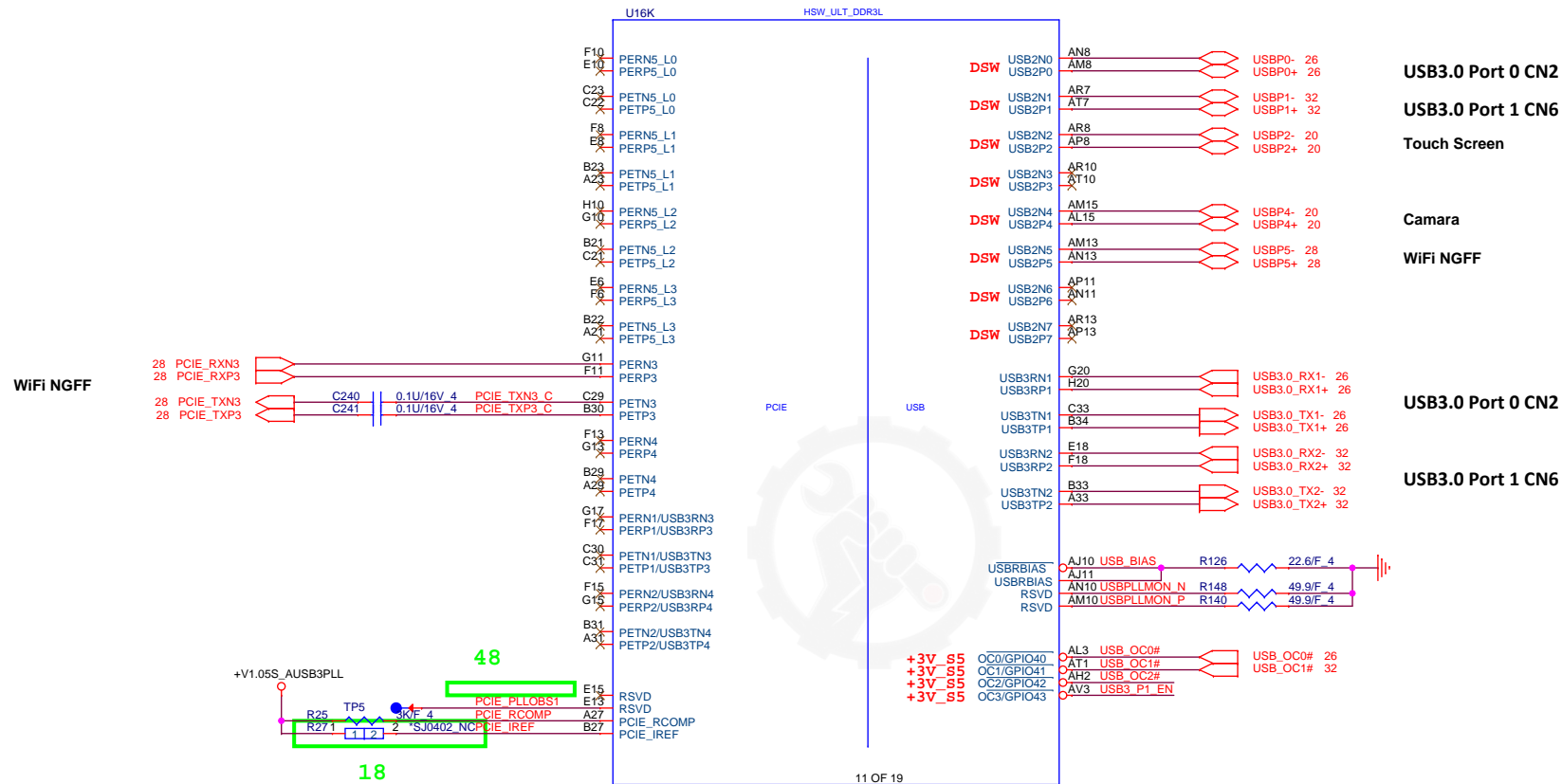
No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

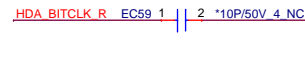
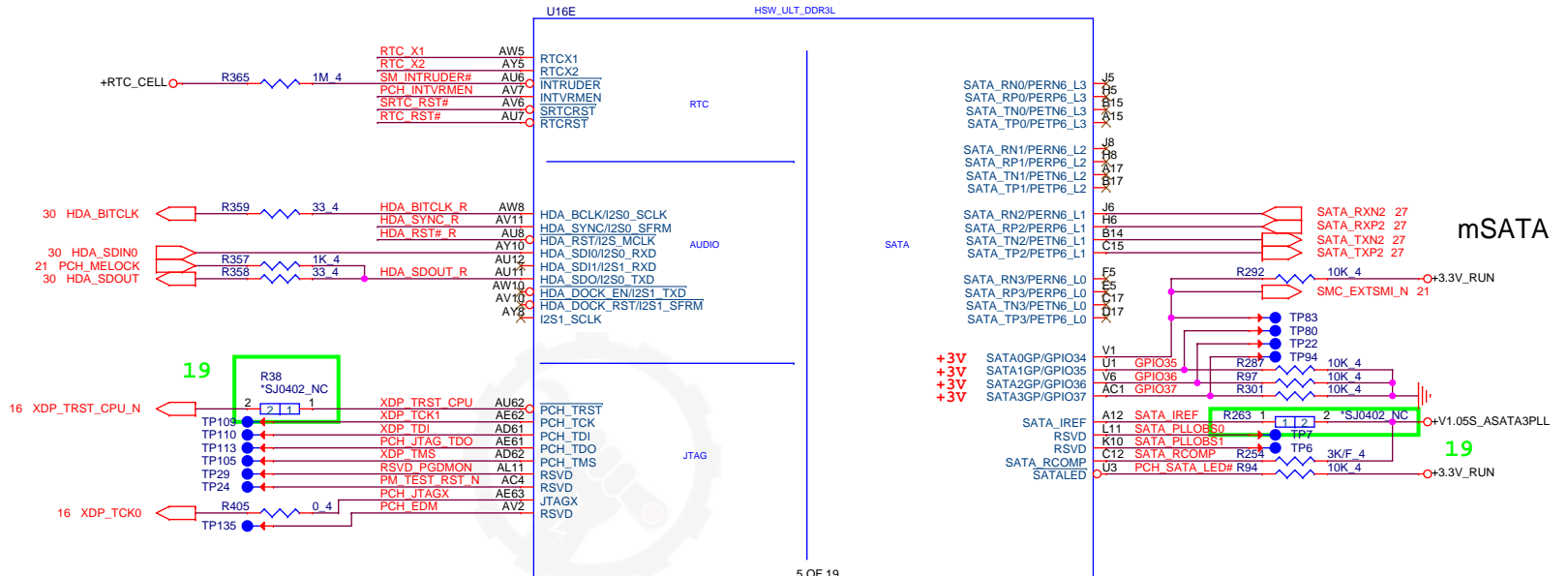
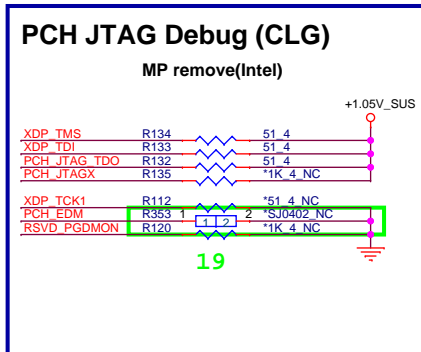
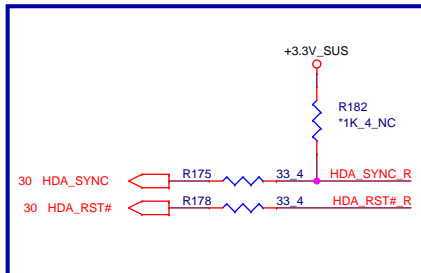
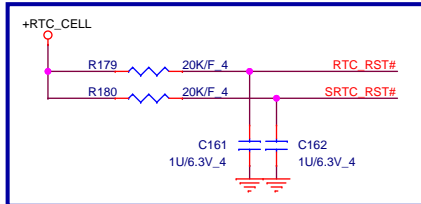
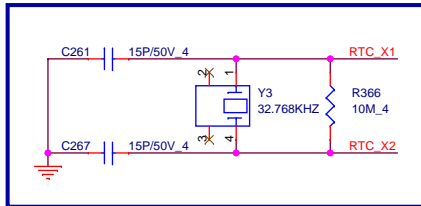
GPIO86	
PU	LPC
PD	SPI (Default)

RAM Vendor select				
RAM Select				
	GPIO90	GPIO91	GPIO92	GPIO93
Micron 4G	0	0	0	0
Micron 8G	0	0	0	1
Hynix 4G	0	1	1	0
Hynix 8G	0	1	1	1
SAM 4G	0	0	1	0

Haswell ULT (PCIE,USB)

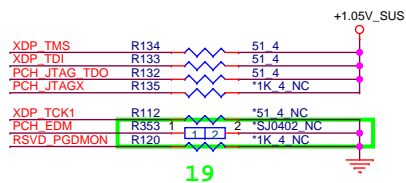


Haswell ULT (RTC, HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

MP remove(Intel)



PCH Strap Table

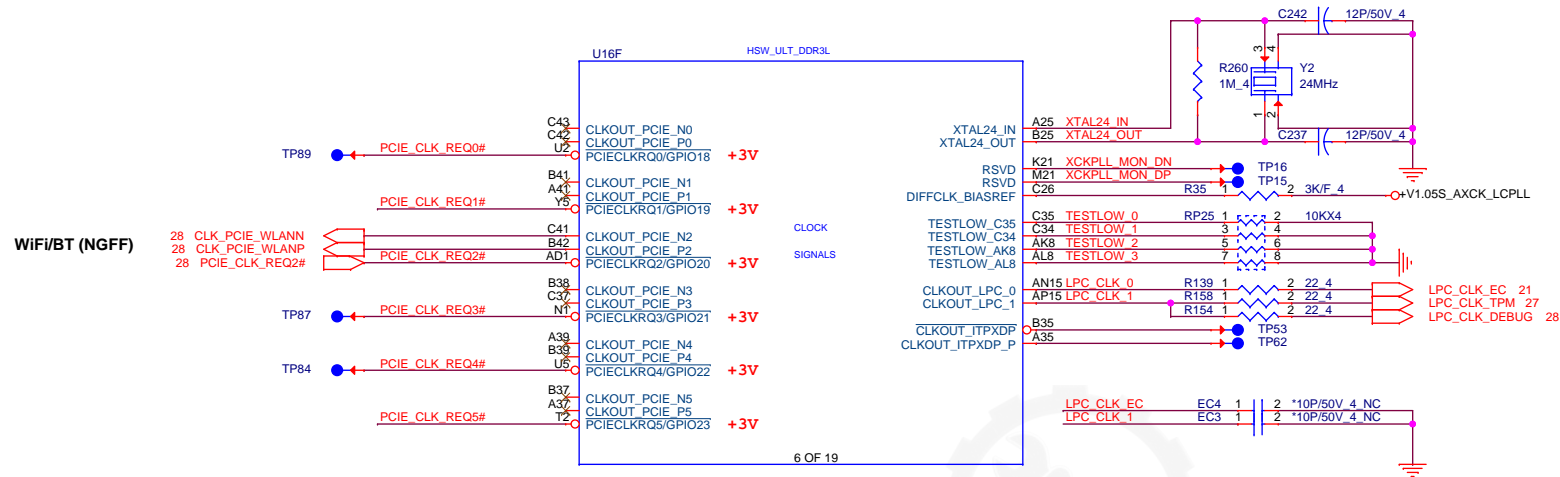
Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R361 *330K 4 NC PCH_INTVRMEN R360 330K 4



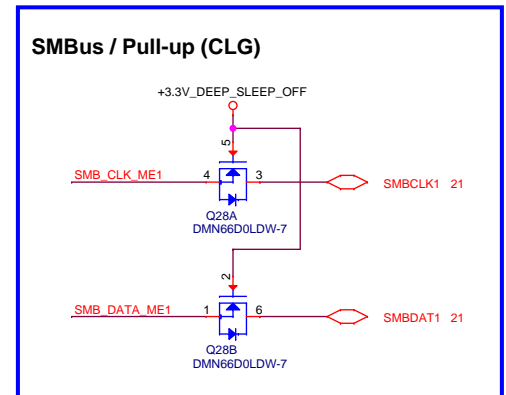
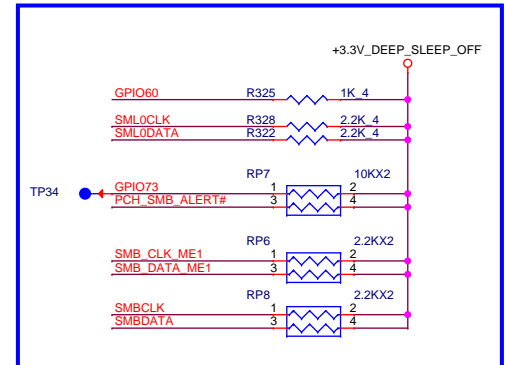
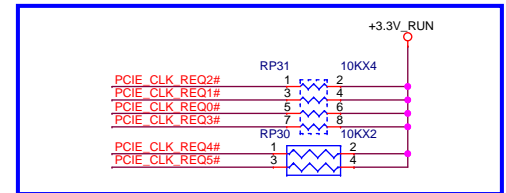
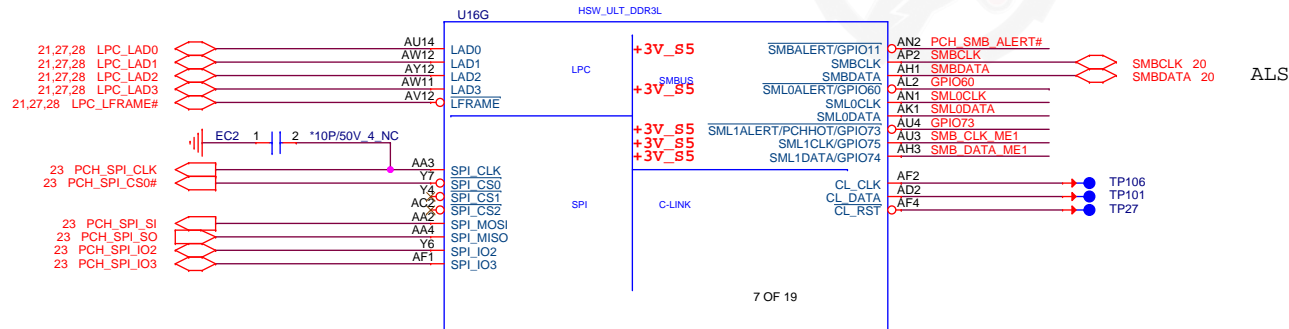
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Haswell ULT (CLK)



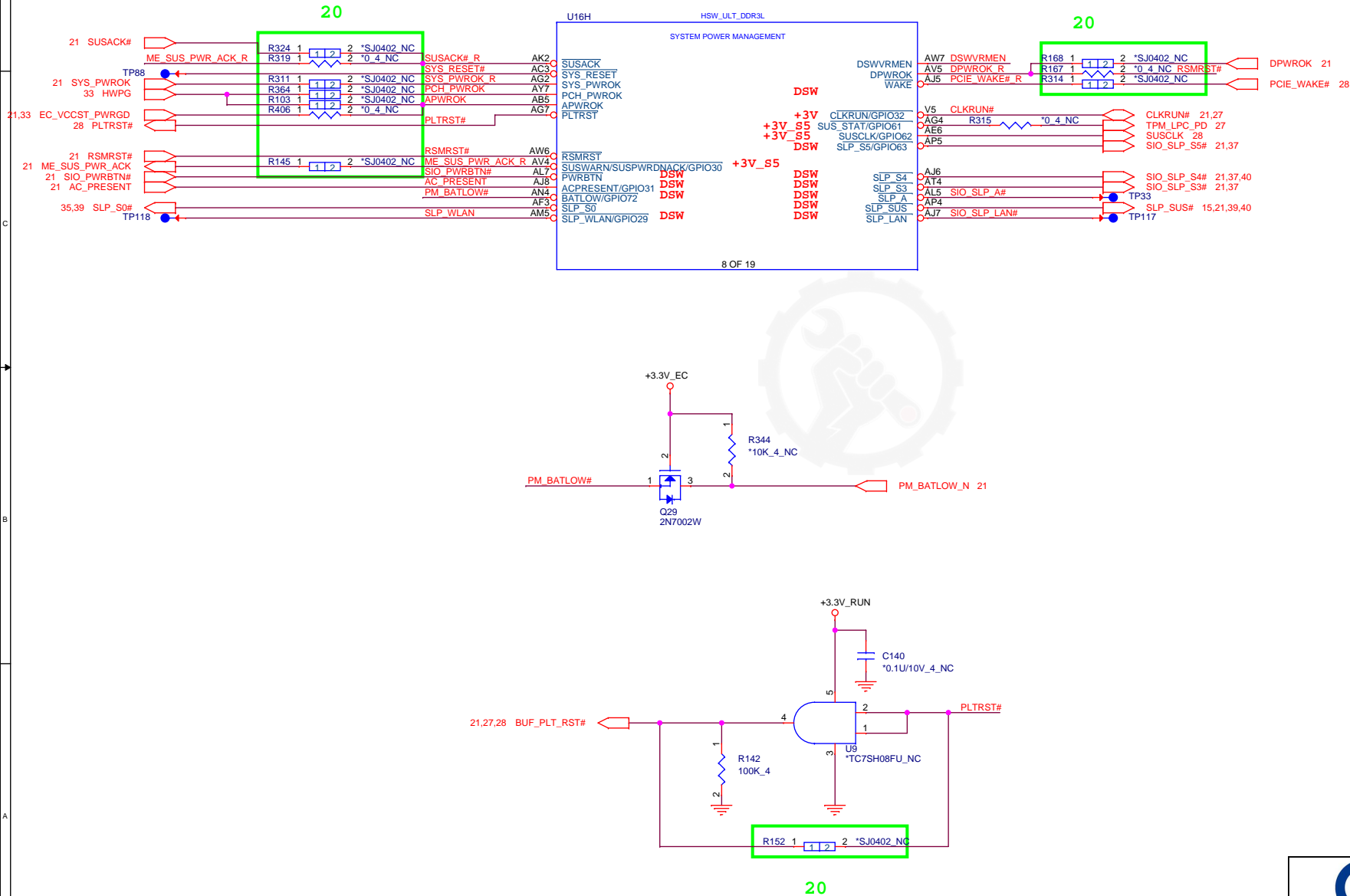
Haswell ULT (LPC/SPI/SMB/CLINK)



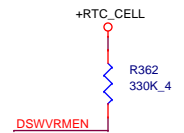
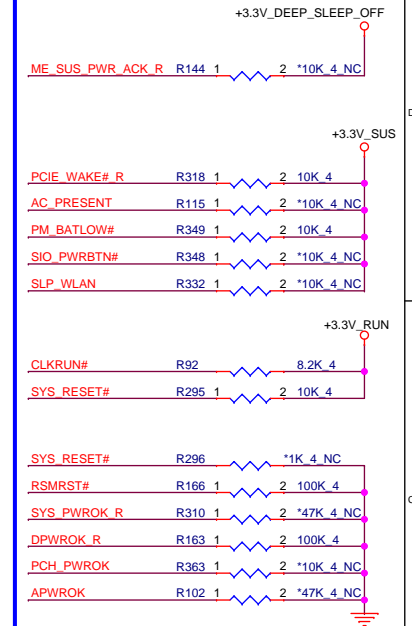
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PROJECT :D13C

Haswell ULT (SYSTEM POWER MANAGEMENT)

Vinafix.com



PCH Pull-up/down (CLG)



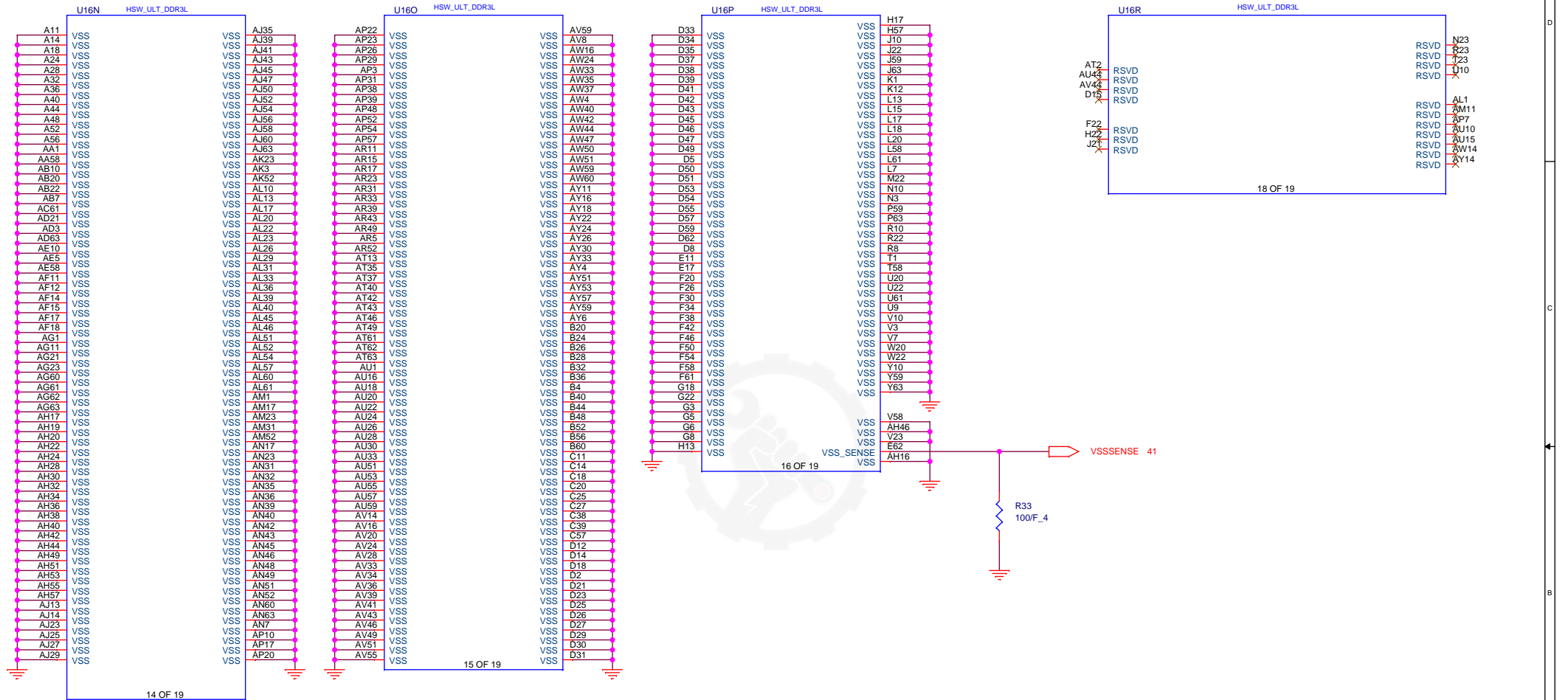
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

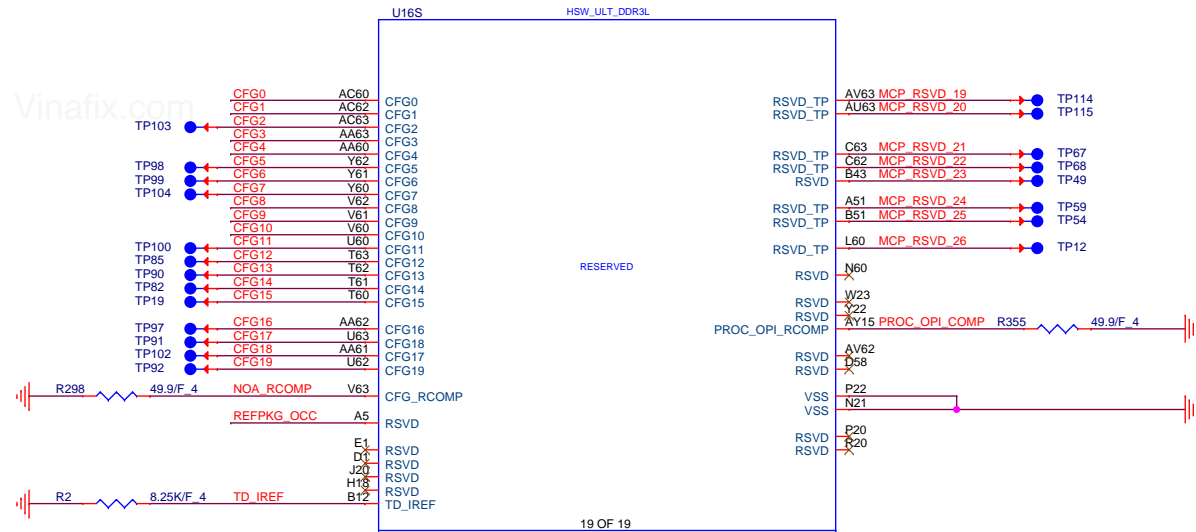


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Haswell ULT (GND)

Vinafix.com





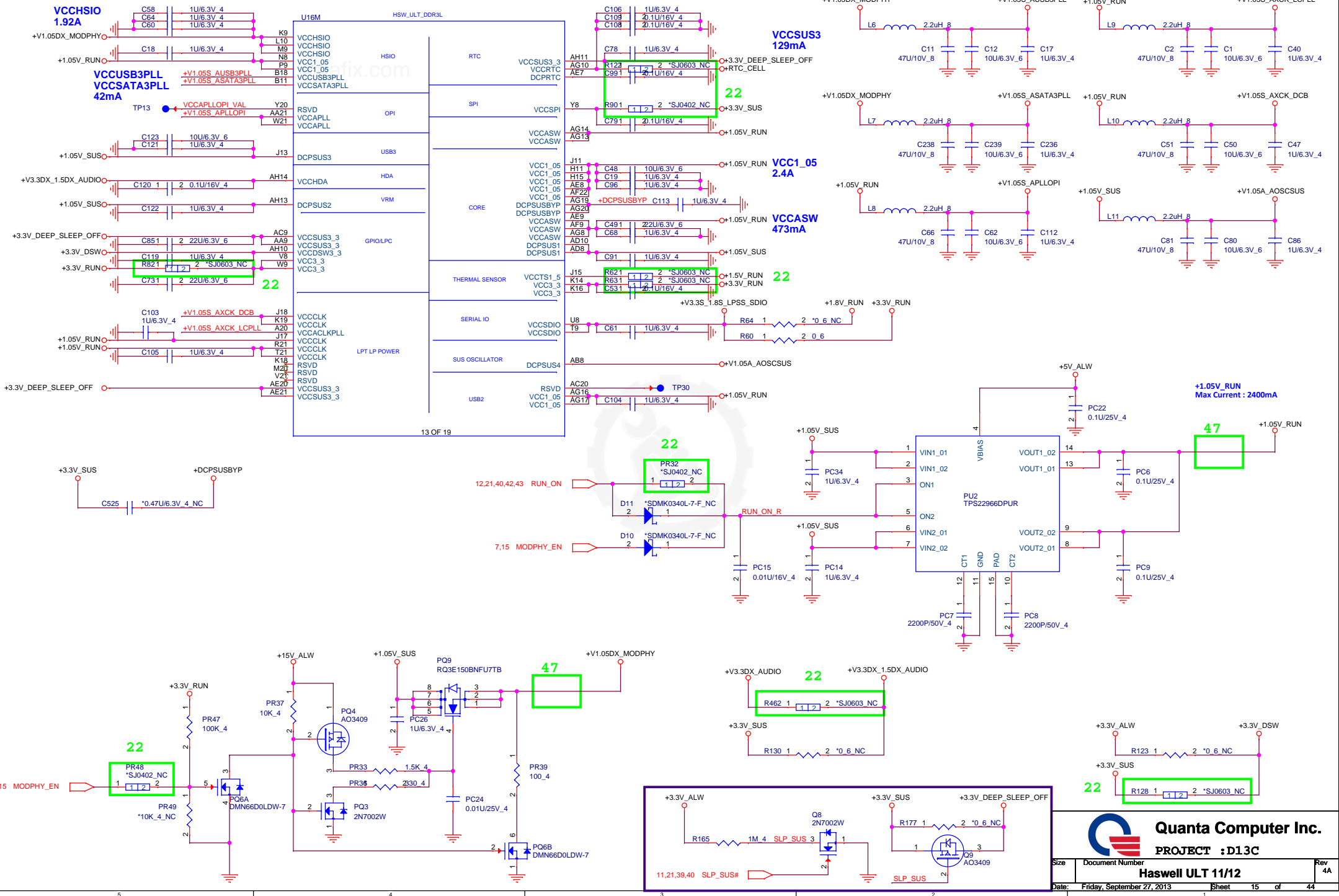
Processor Strapping

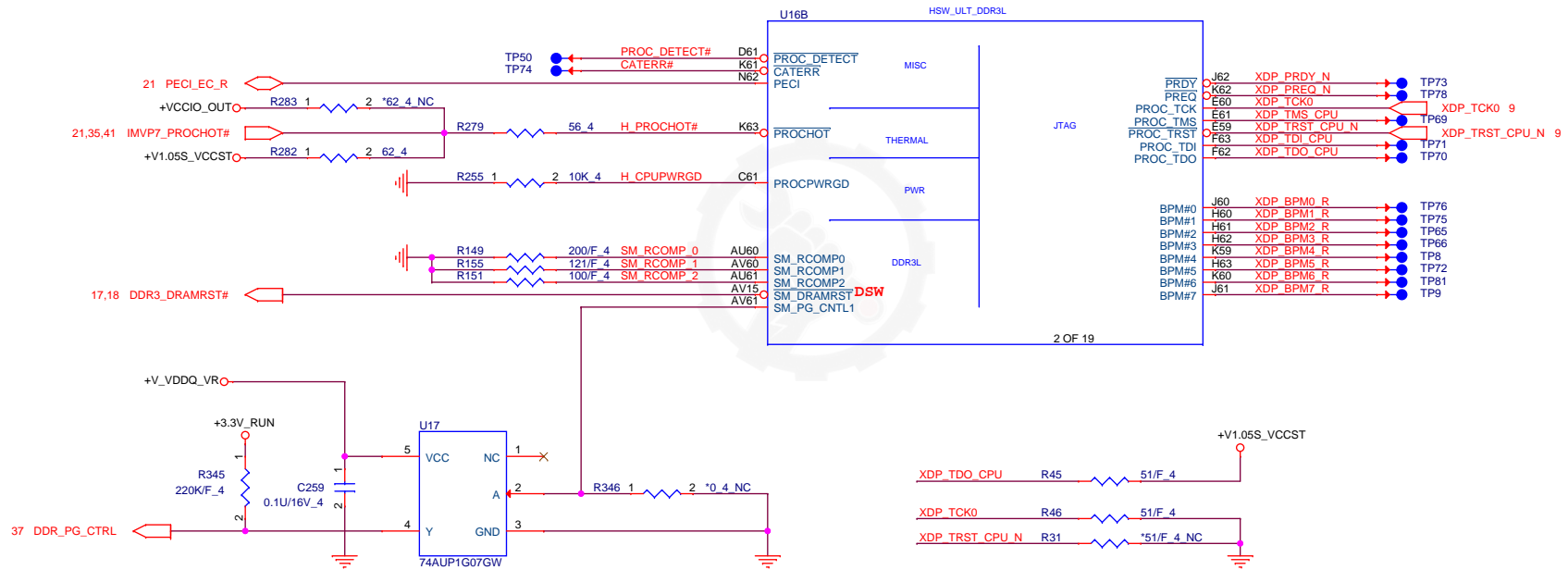
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R117 *1K 4 NC
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R109 *1K 4 NC
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R300 *1K 4 NC
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R101 1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R88 *1K 4 NC
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R83 *1K 4 NC
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R96 *1K 4 NC
REFPKG_OCC SIGNAL USAGE	OPEN NORMAL HSW ULT PACKAGE	GND HSW INTERPOSTER	+3.3V_RUN REFPKG_OCC R265 1 *100K/F 4 NC



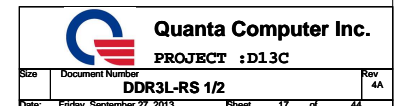
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PROJECT :D13C

Haswell ULT PCH(POWER)



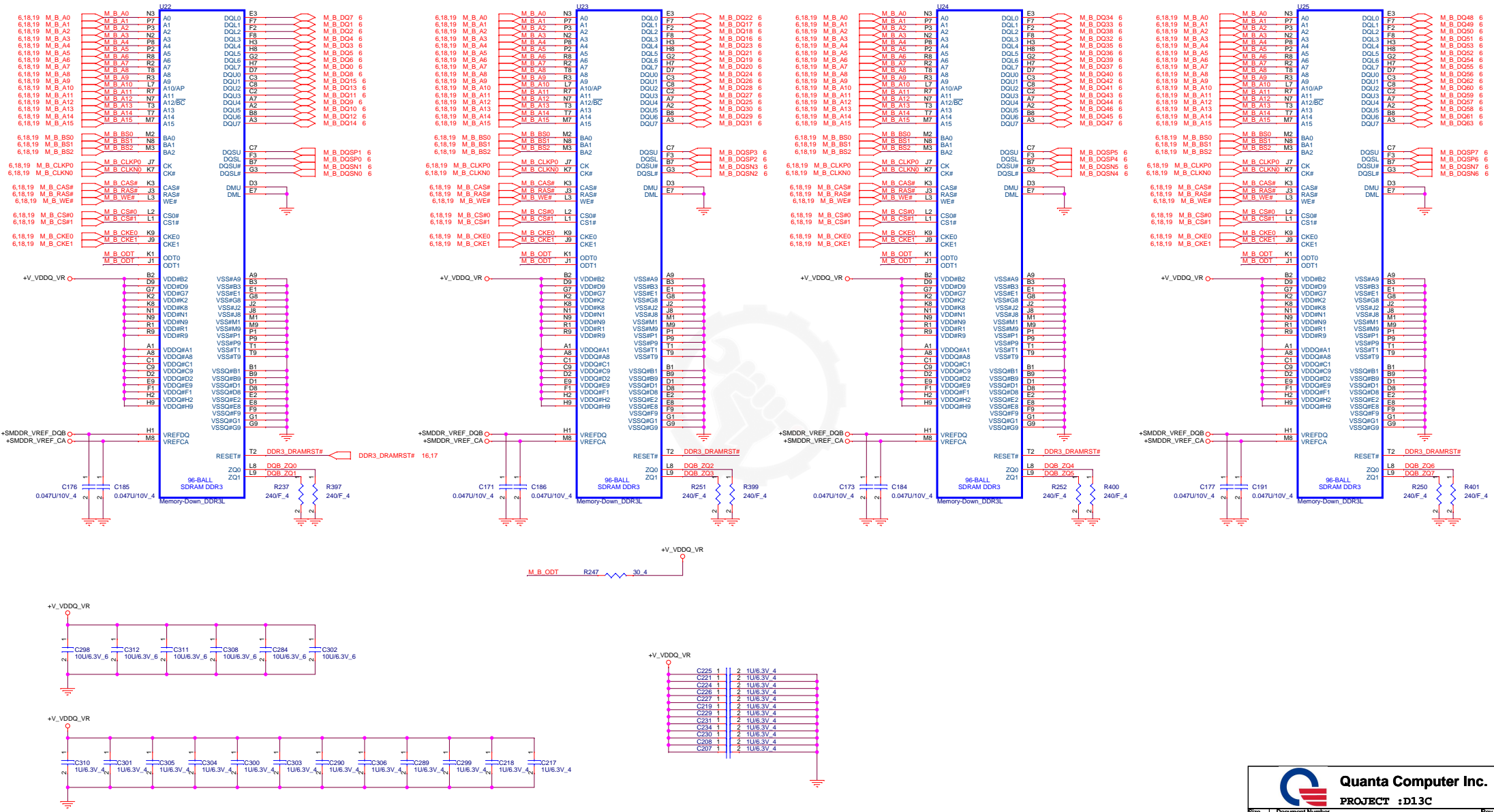


Quanta Computer Inc.
PROJECT :D13C

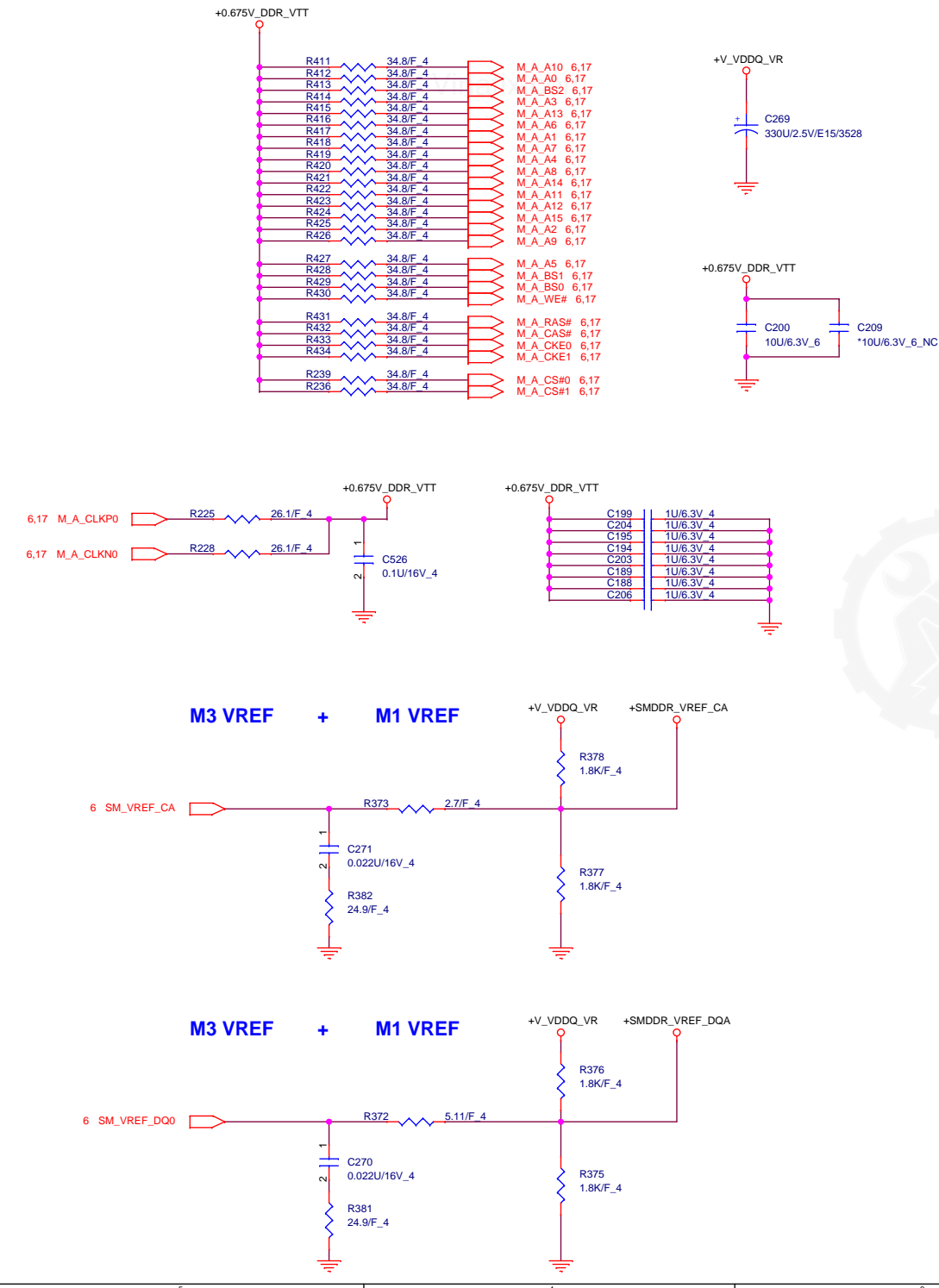


Channel B: 512Mb*16 DDR3L-RS
256Mb*16 DDR3L-RS

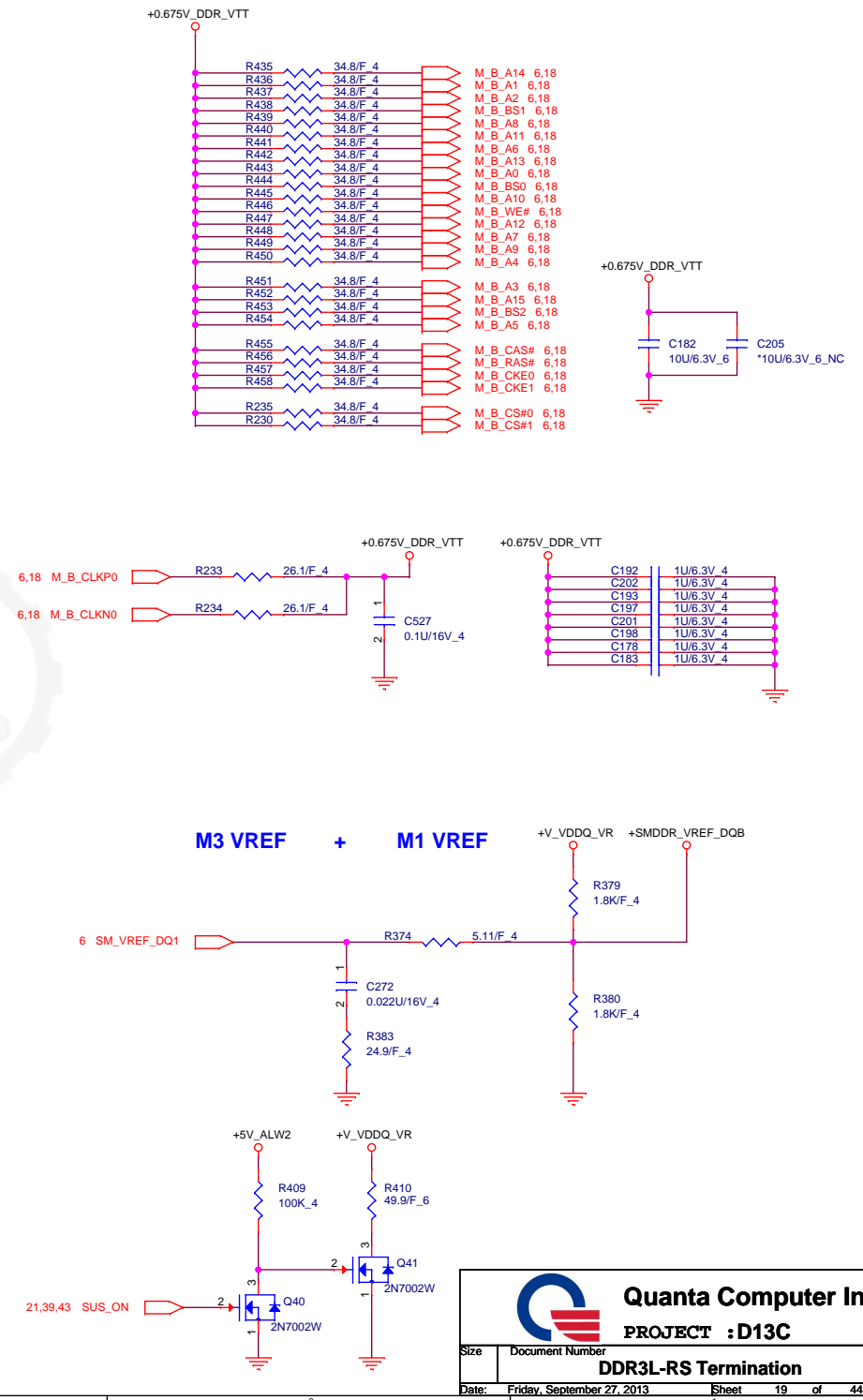
Vinafix.com



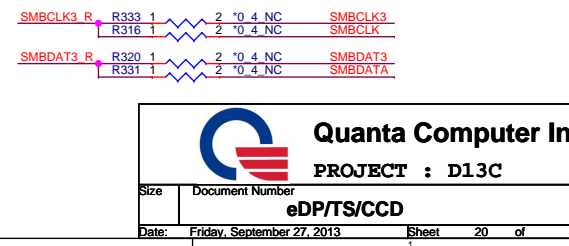
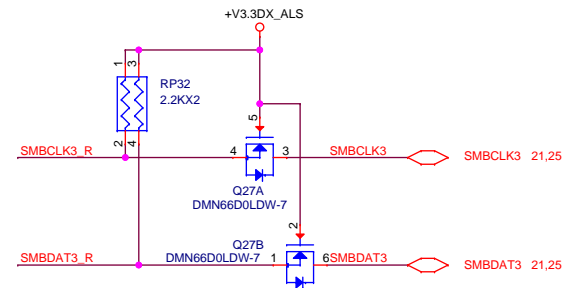
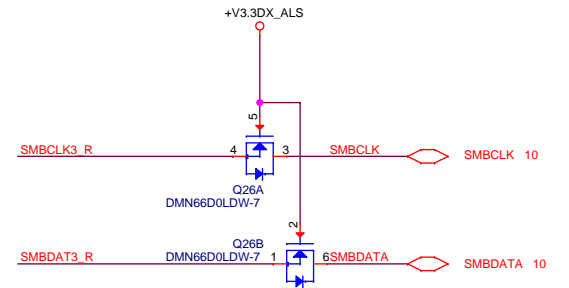
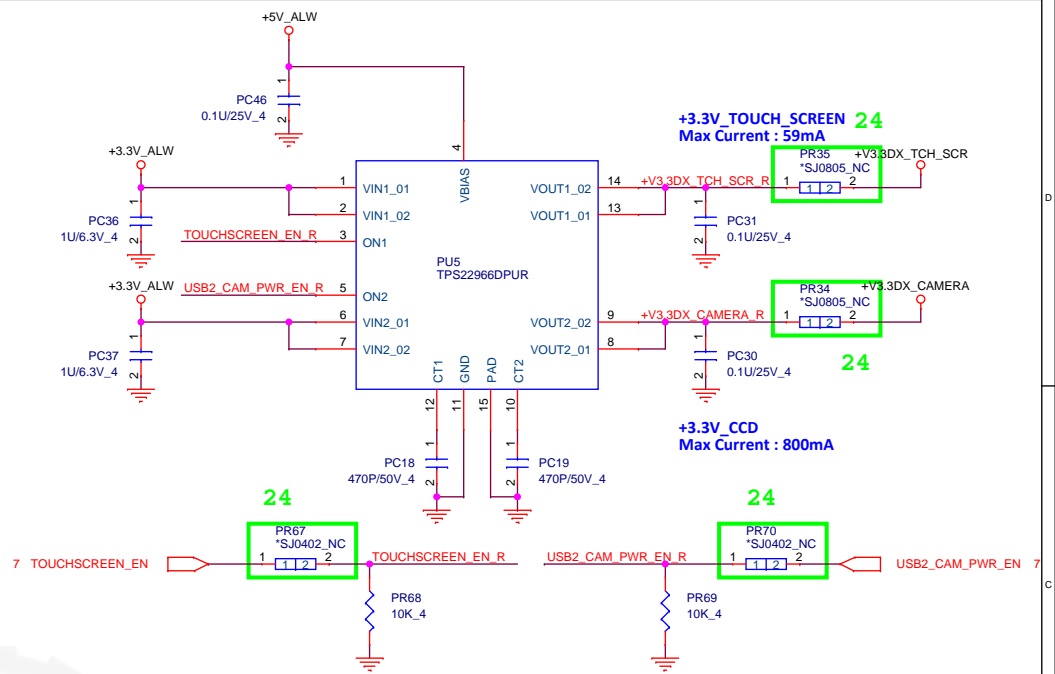
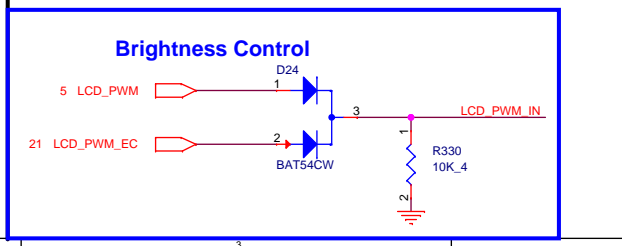
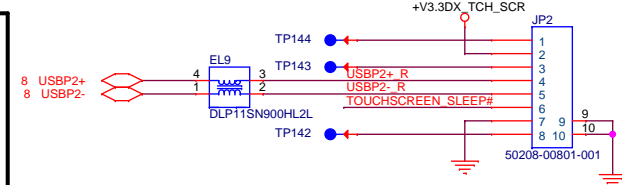
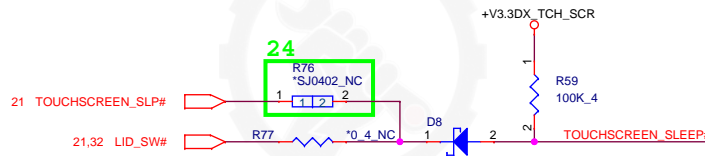
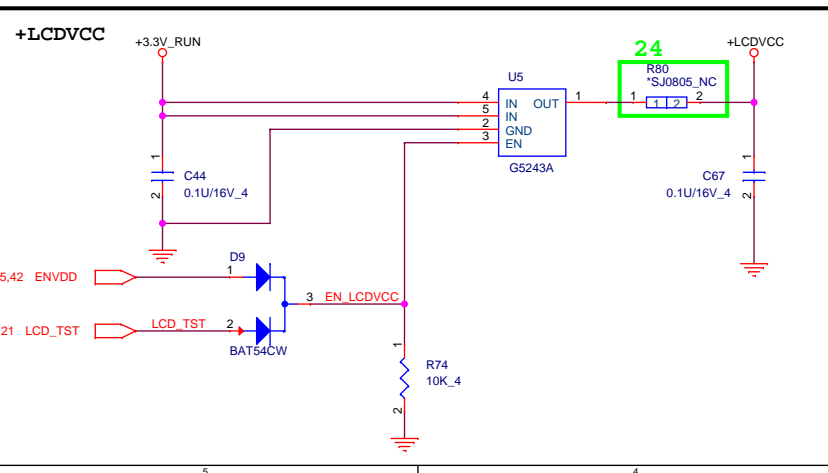
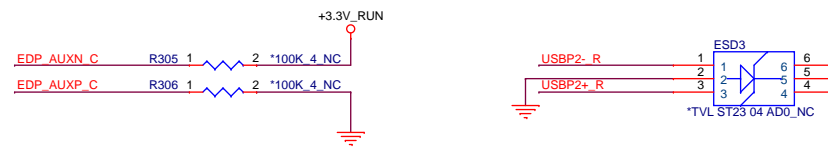
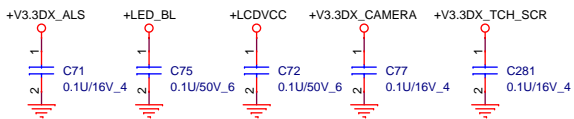
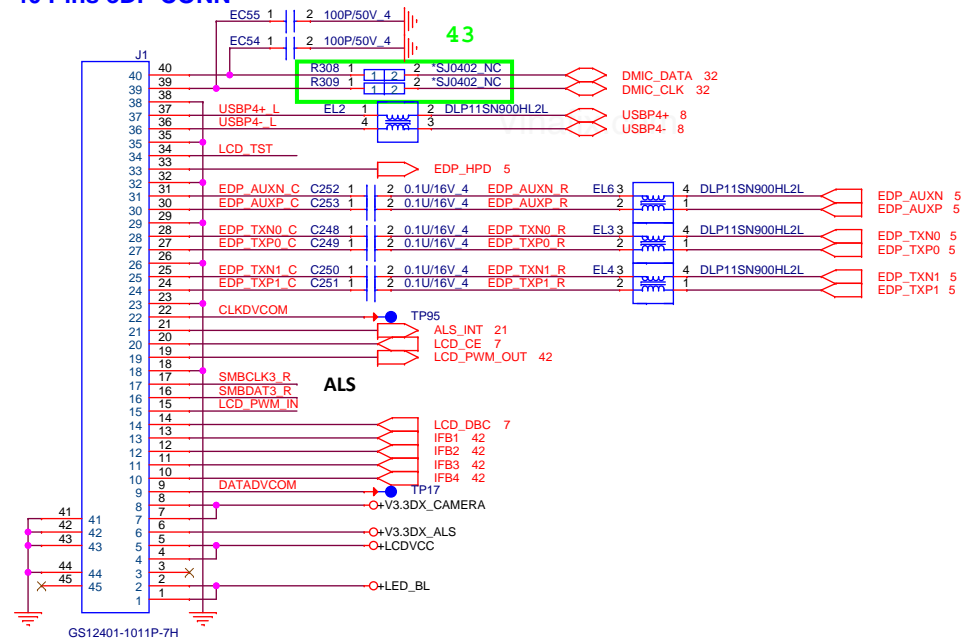
Channel A

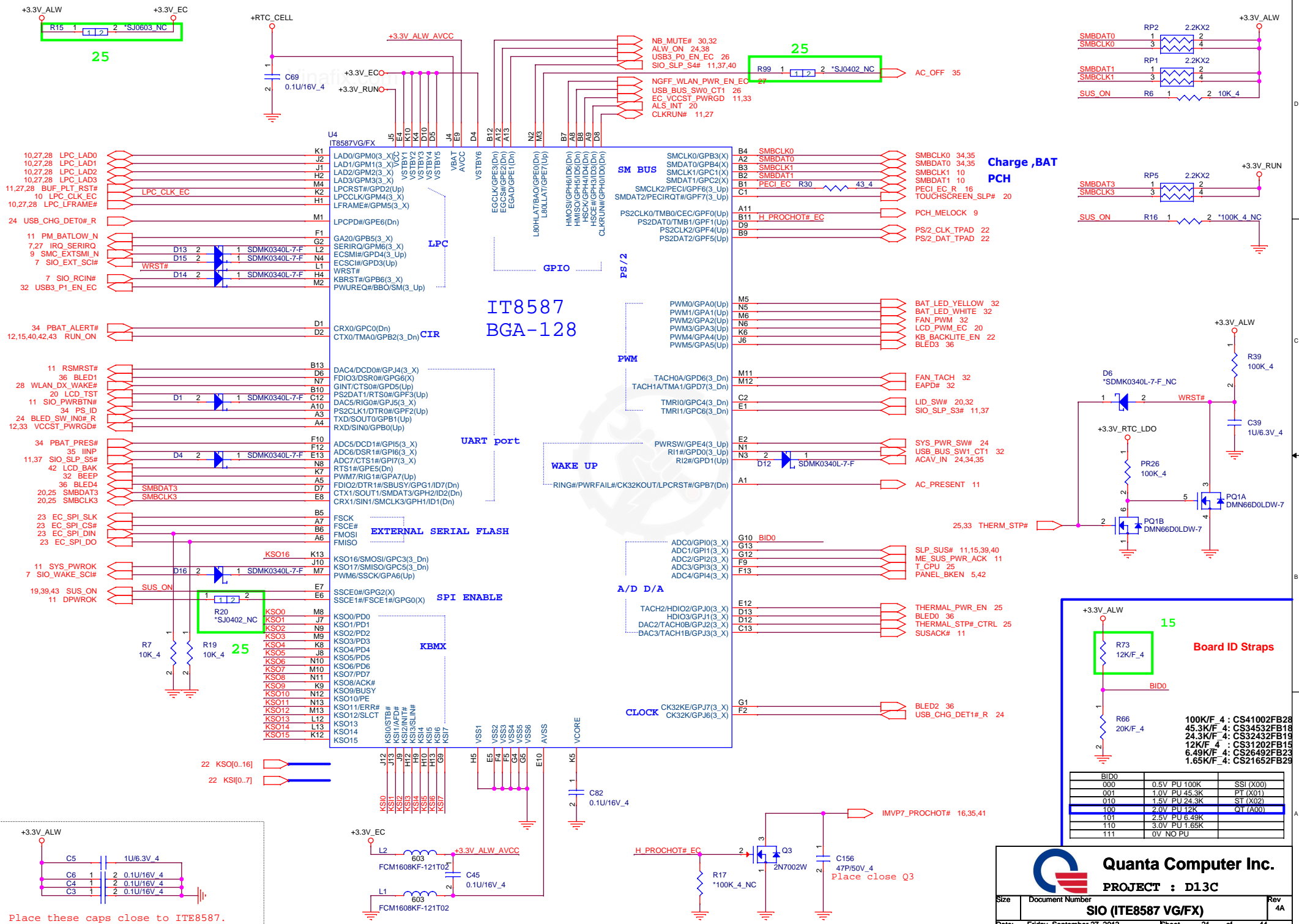


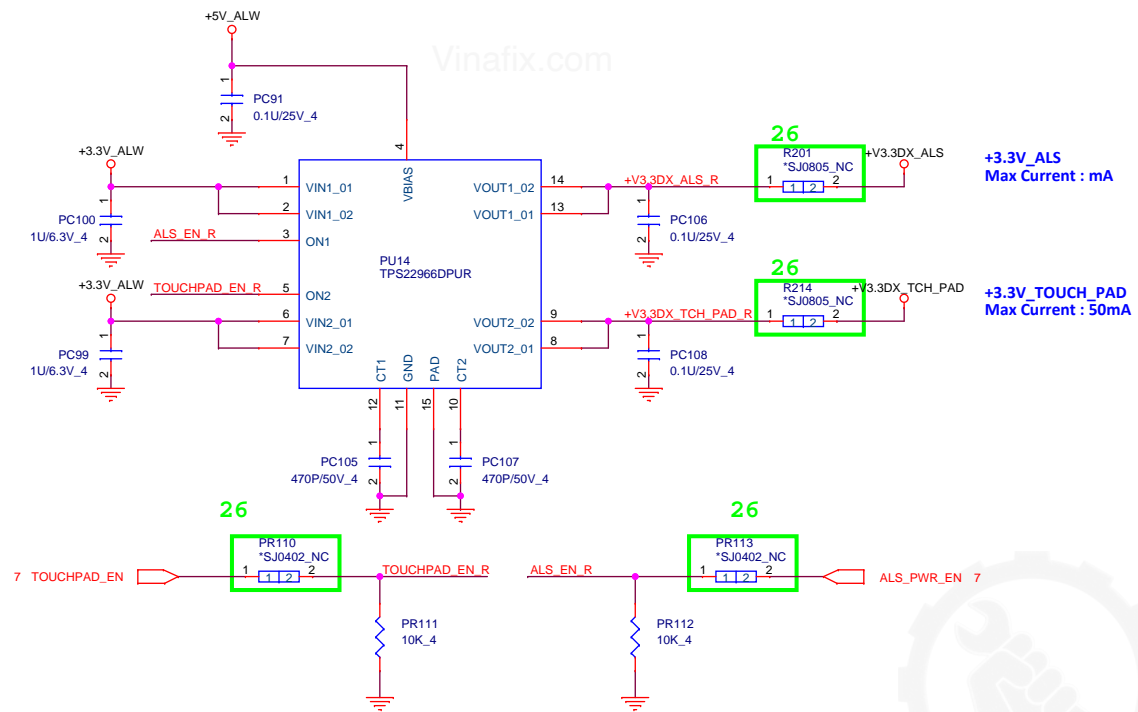
Channel B



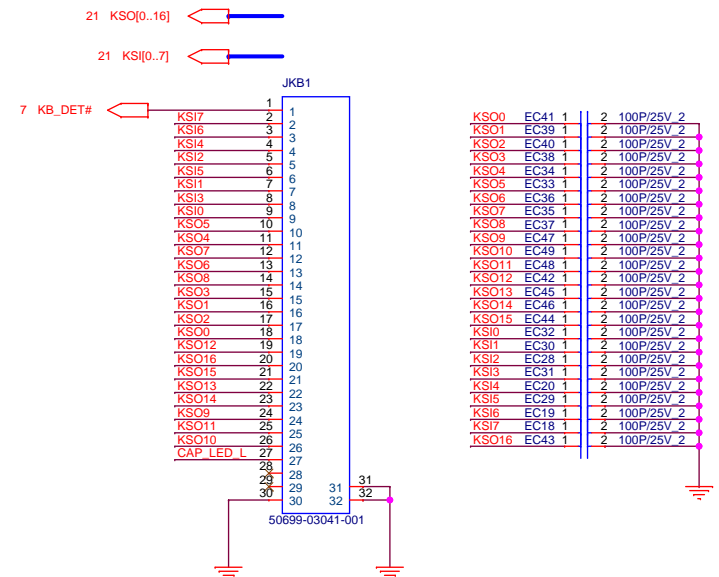
40 Pins eDP CONN



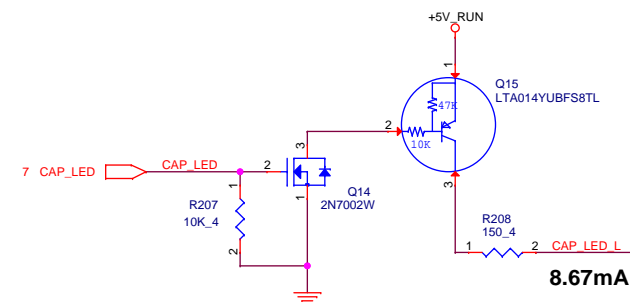
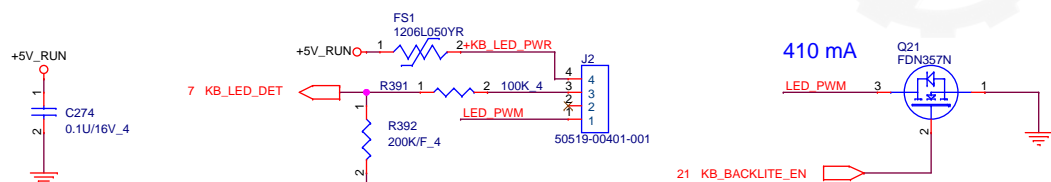




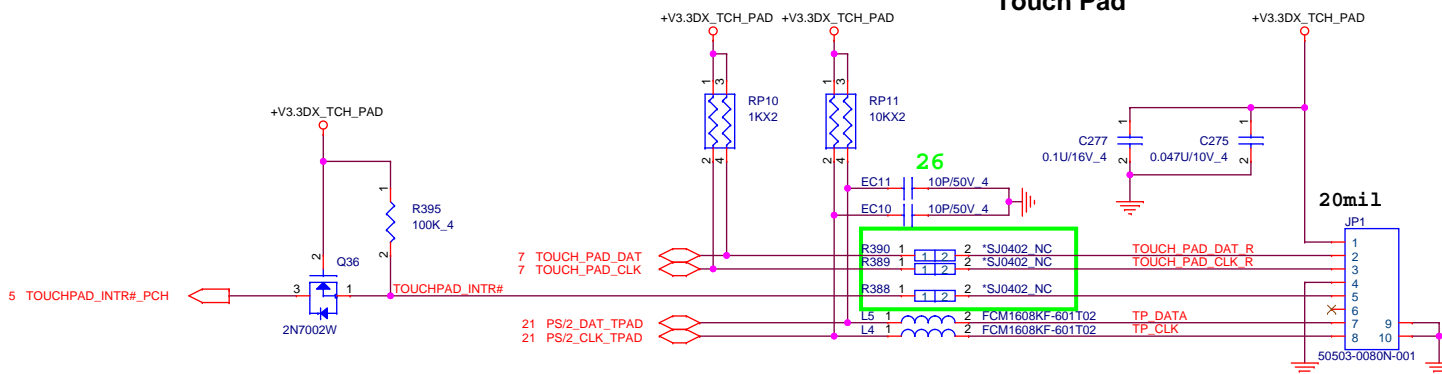
Keyboard Connector



Key board illumination



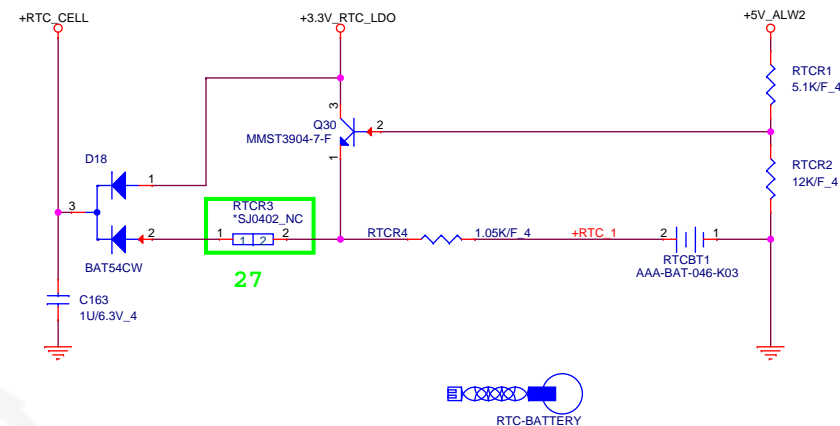
Touch Pad



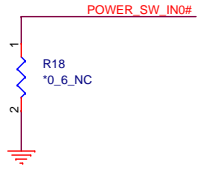
Quanta Computer Inc.
PROJECT : D13C



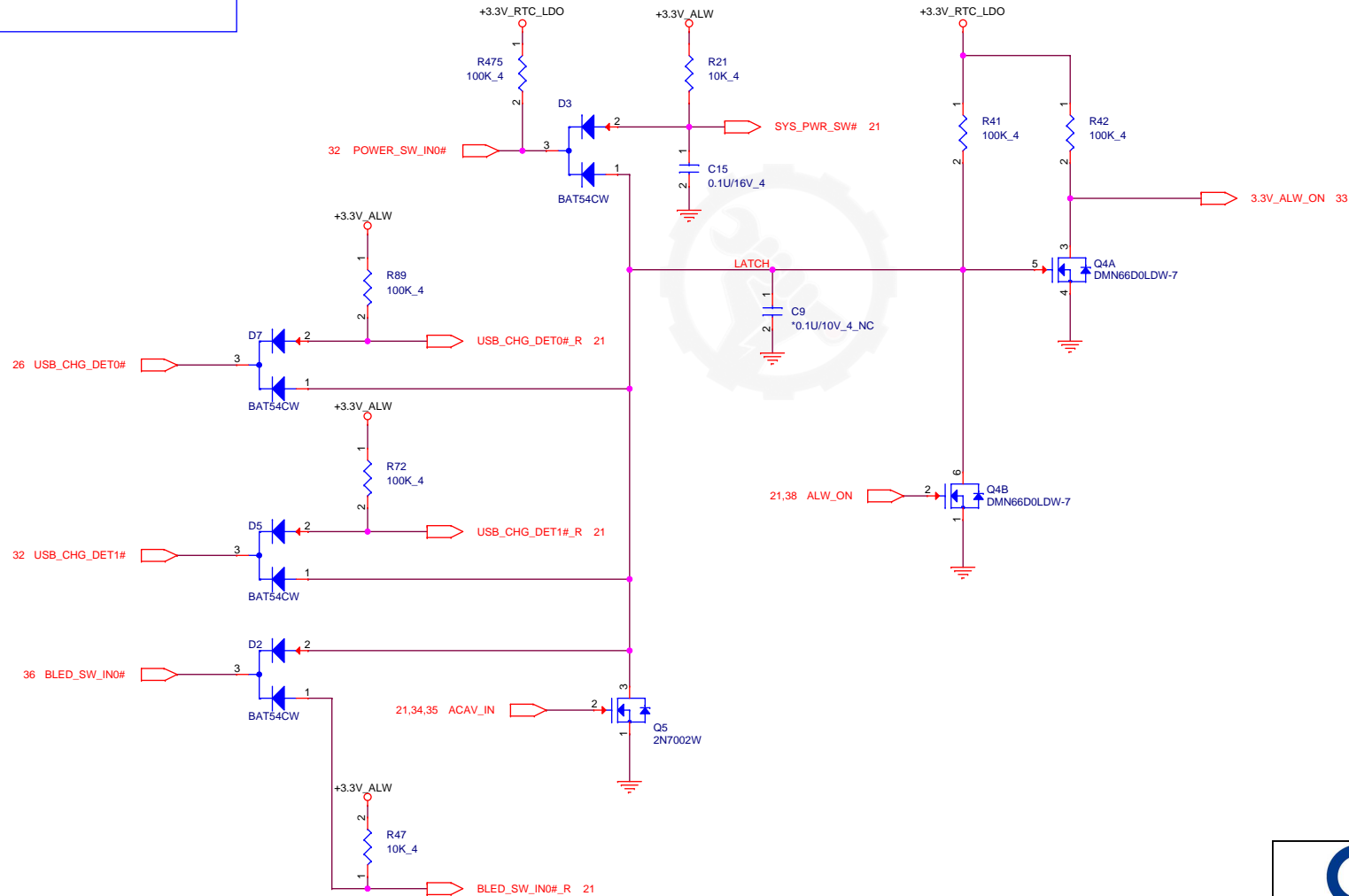
RTC Battery



For Debug PWR SW



3VALW ON POWER LOGIC

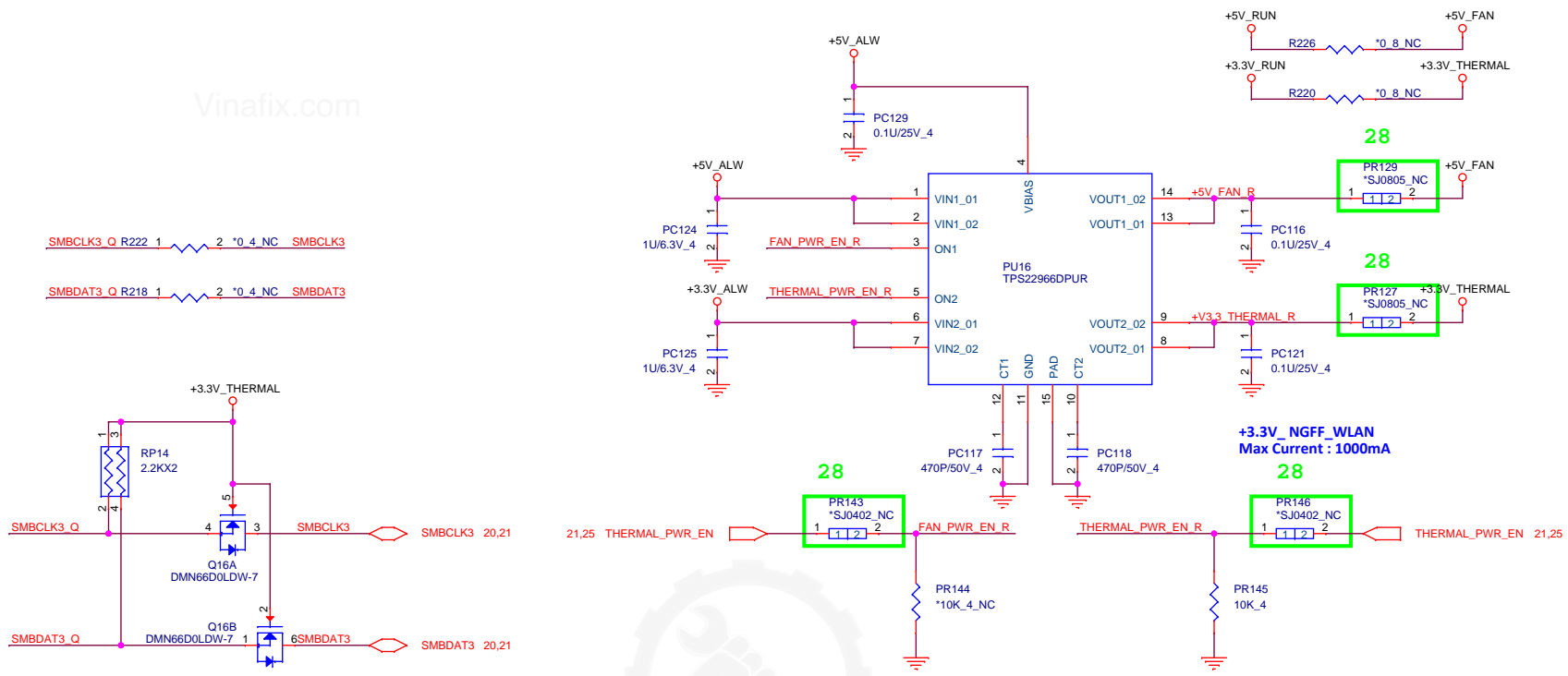


Quanta Computer Inc.

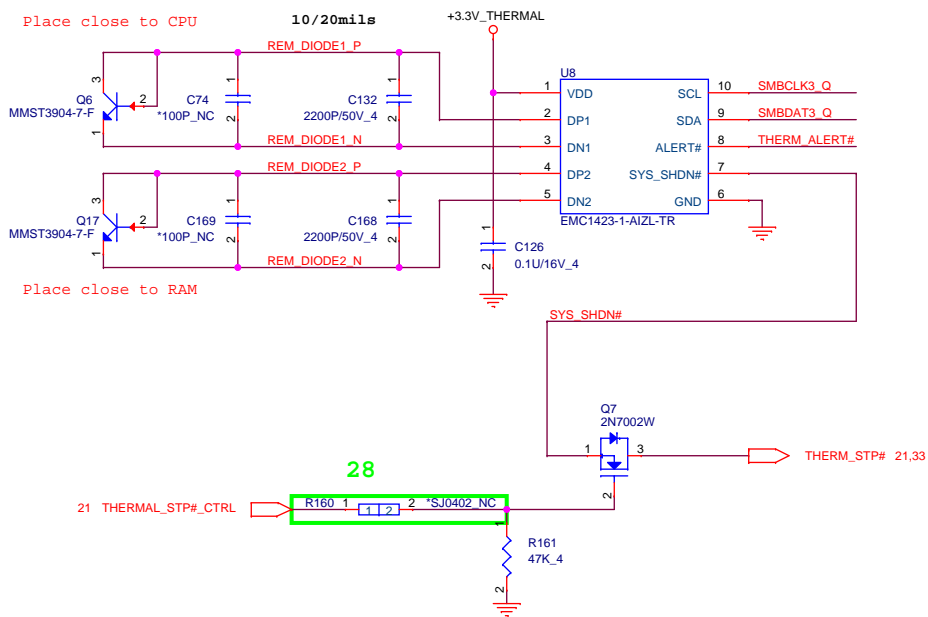
PROJECT : D13C

Size	Document Number	Rev
		4A
Date:	Friday, September 27, 2013	Sheet 24 of 44

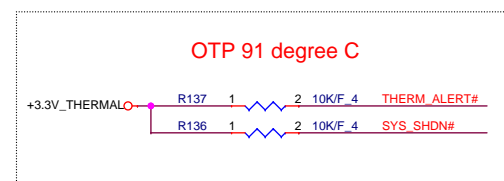
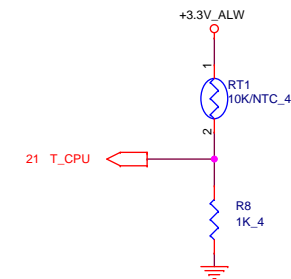
3VALW ON POWER LOGIC

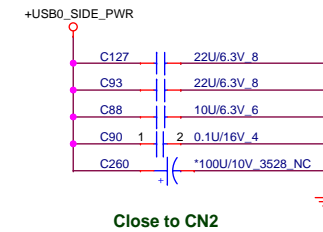
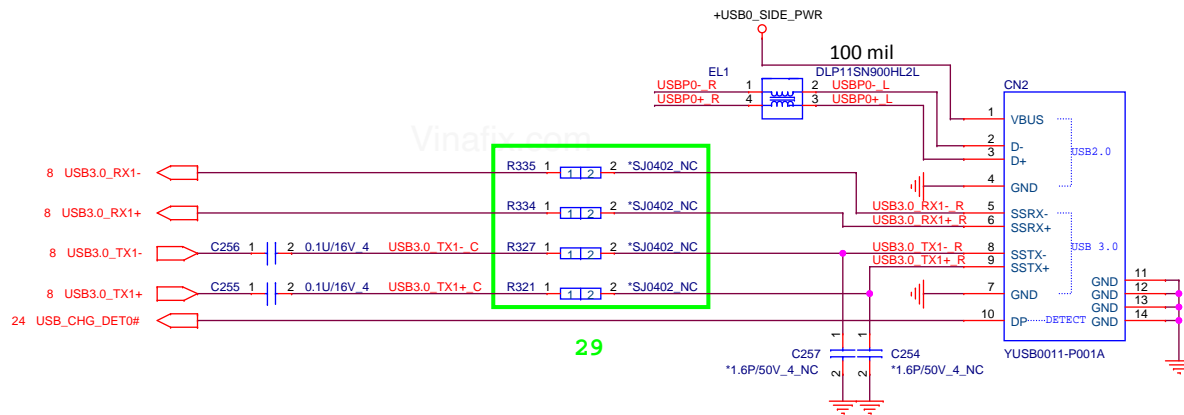


THERMAL IC



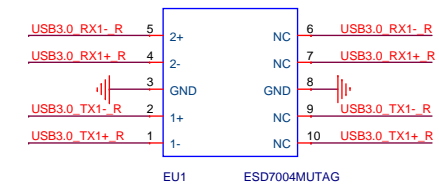
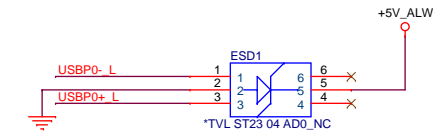
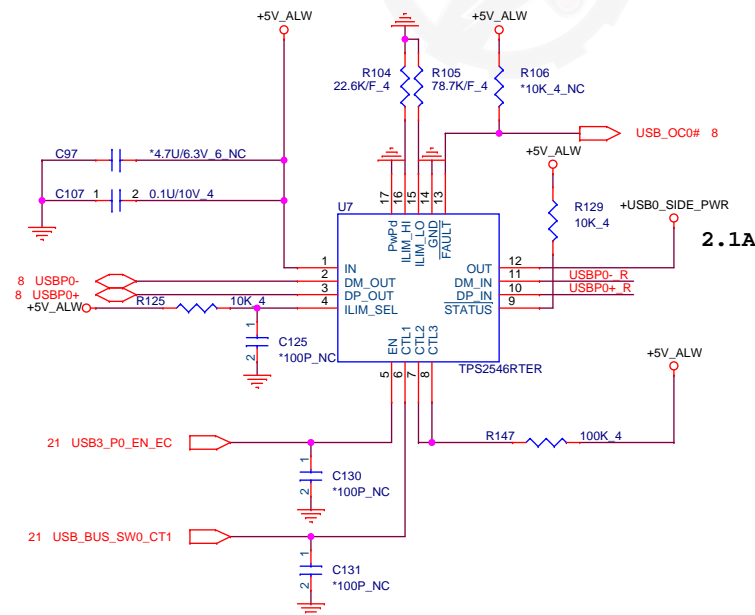
SYS_SHDN#	4.7K	6.8K	10K	15K	22K	33K
ALERT#						
4.7K	77 °C	83 °C	89 °C	95 °C	101 °C	107 °C
6.8K	78 °C	84 °C	90 °C	96 °C	102 °C	108 °C
10K	79 °C	85 °C	91 °C	97 °C	103 °C	109 °C
15K	80 °C	86 °C	92 °C	98 °C	104 °C	110 °C
22K	81 °C	87 °C	93 °C	99 °C	105 °C	111 °C
33K	82 °C	88 °C	94 °C	100 °C	106 °C	112 °C





USB Power share

USB_BUS_SW0_CT1	Mode	Operating at
High	CDP	S0, 1.5 A
Low	DCP, Auto-detect	S3/S4/S5, 2.1/1.5 A

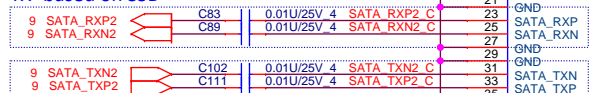


	R104	mA
OC limitation	22.6k ohm	2224
	23.2k ohm	2167

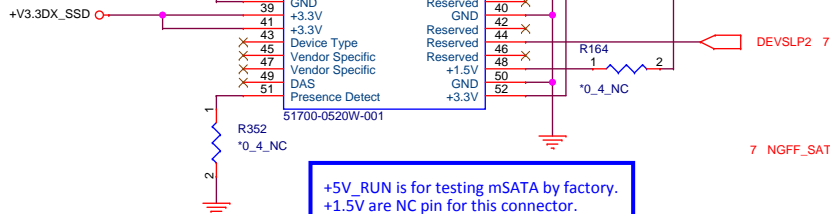
mSATA Connector

Max = 6000 mils
Min = 1000 mils
DG: Place TX cap close to connector

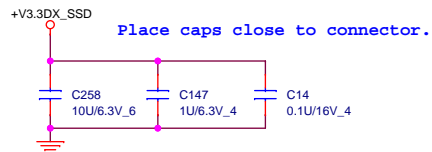
TX- based on SSD



RX- based on SSD

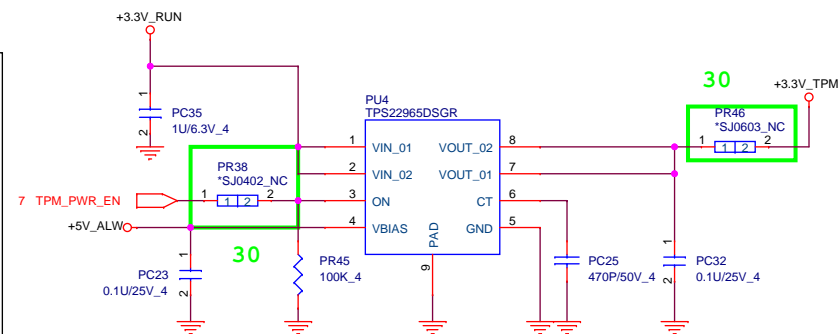
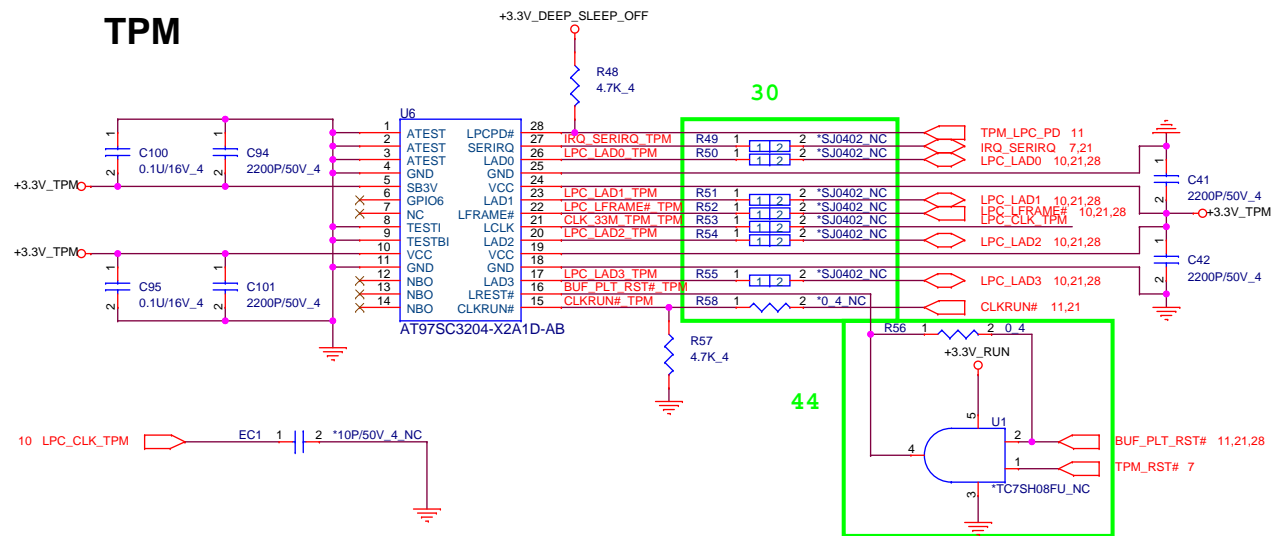


+5V_RUN is for testing mSATA by factory.
+1.5V are NC pin for this connector.

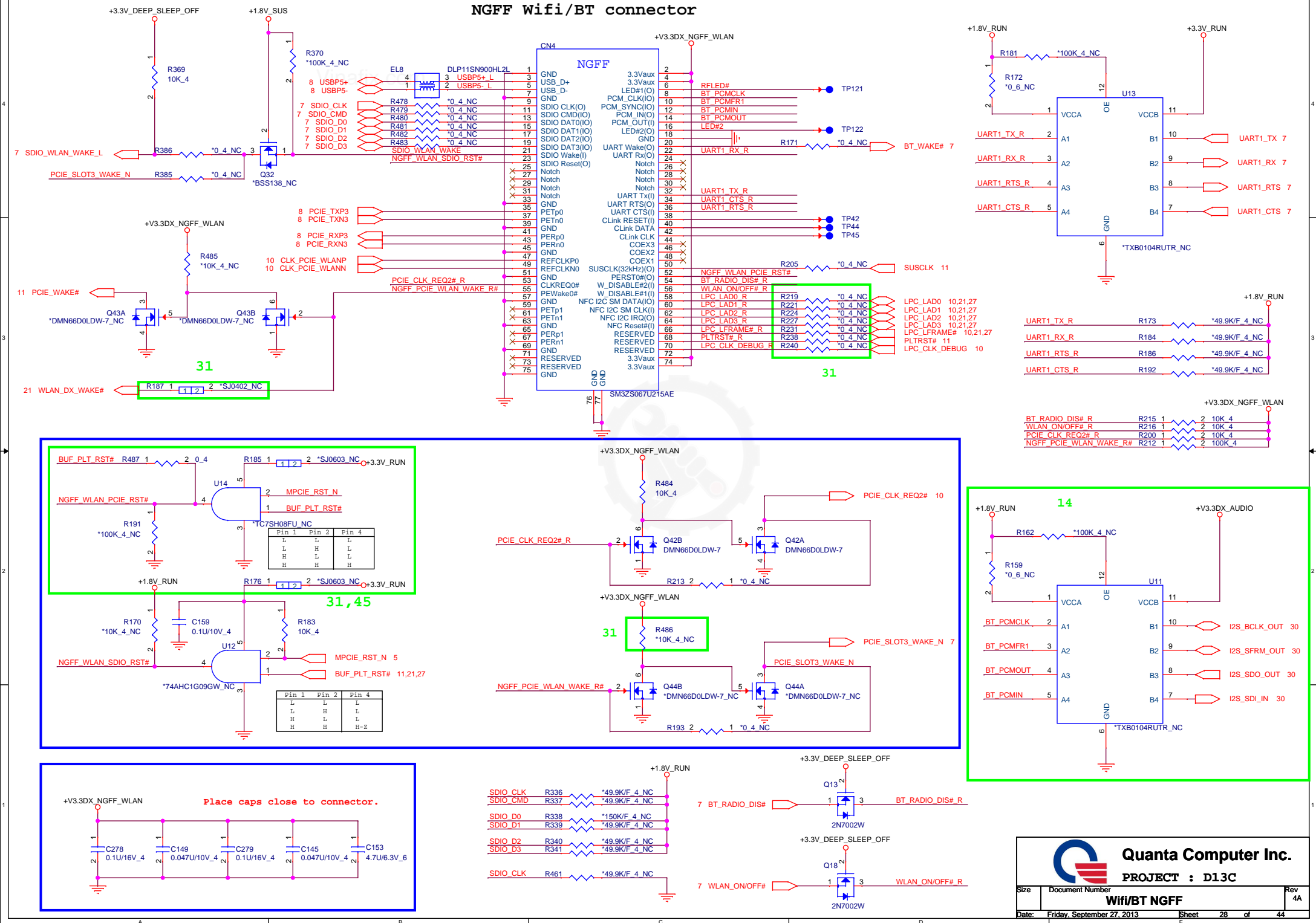


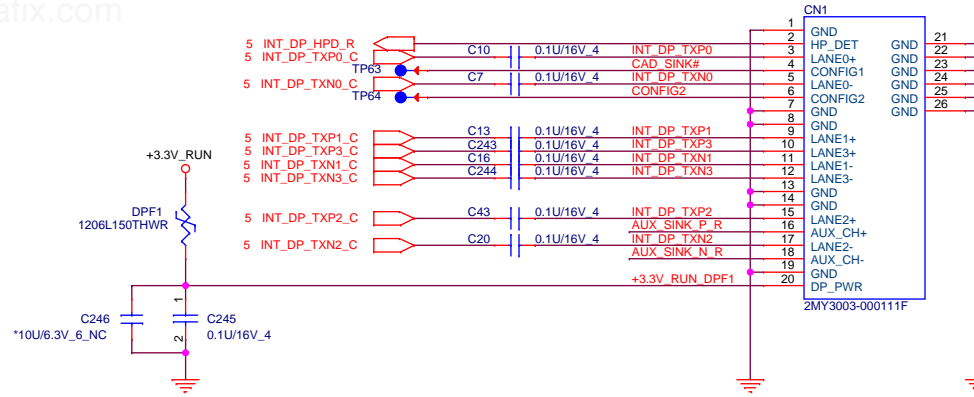
Place caps close to connector.

TPM

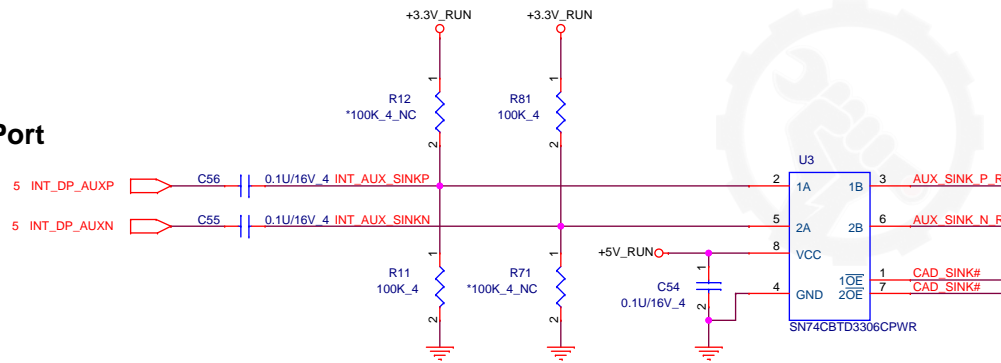


NGFF Wifi/BT connector

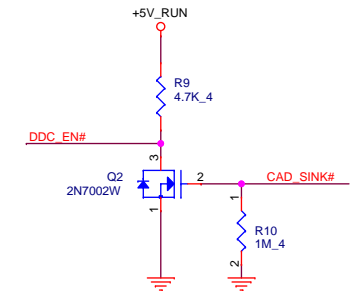
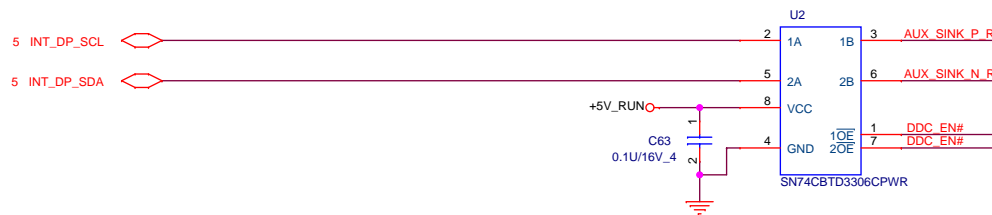




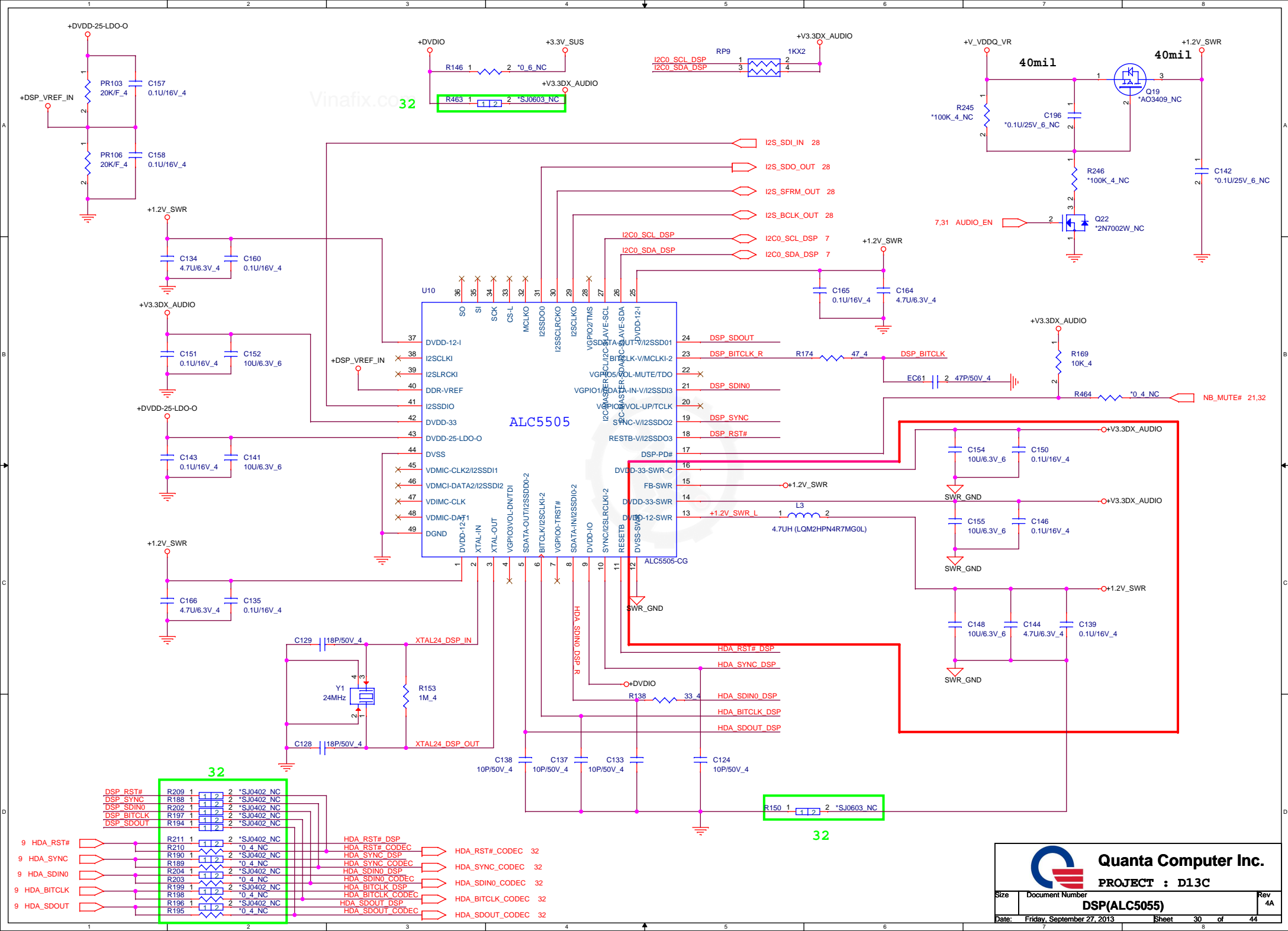
DisplayPort



HDMI

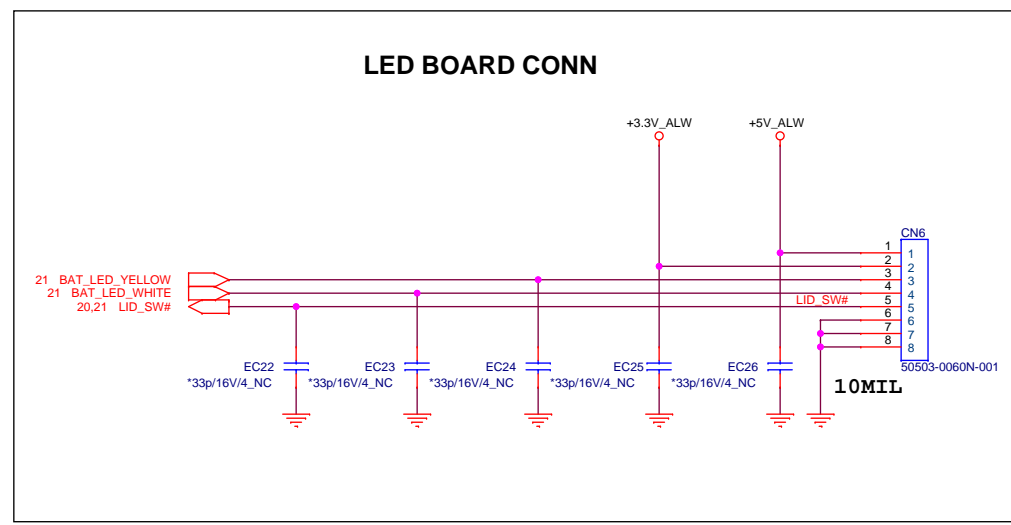
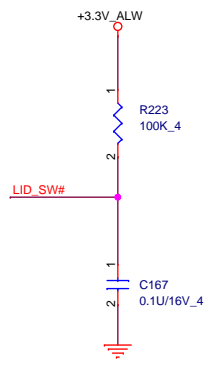
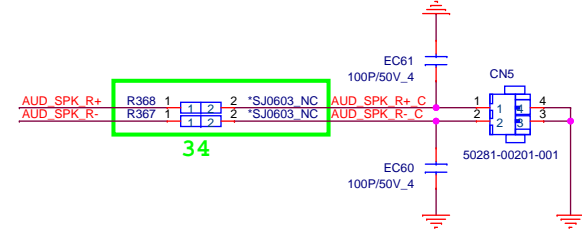
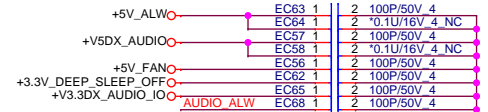
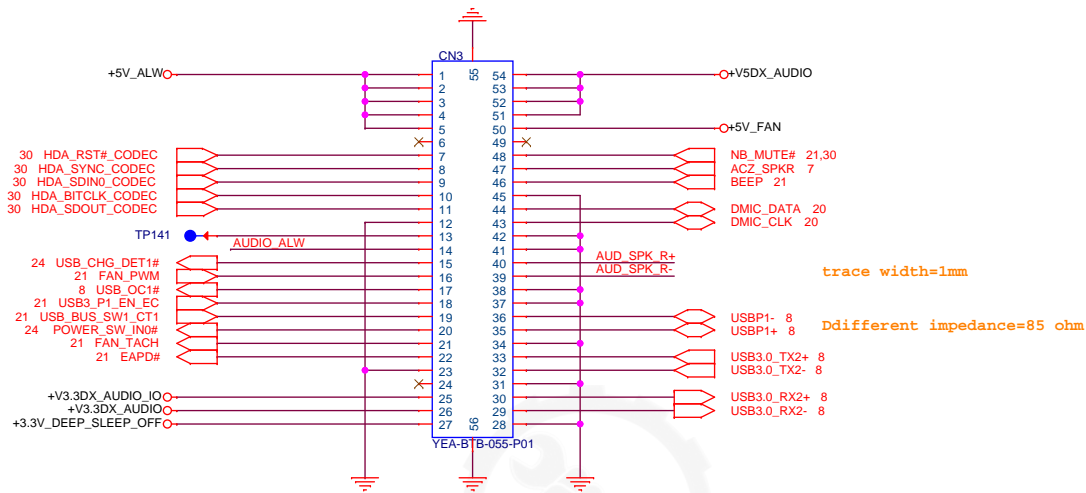
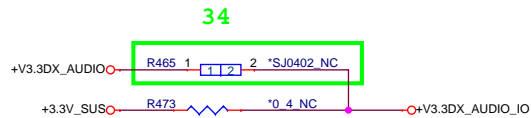
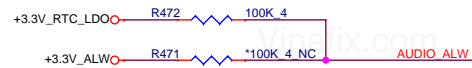


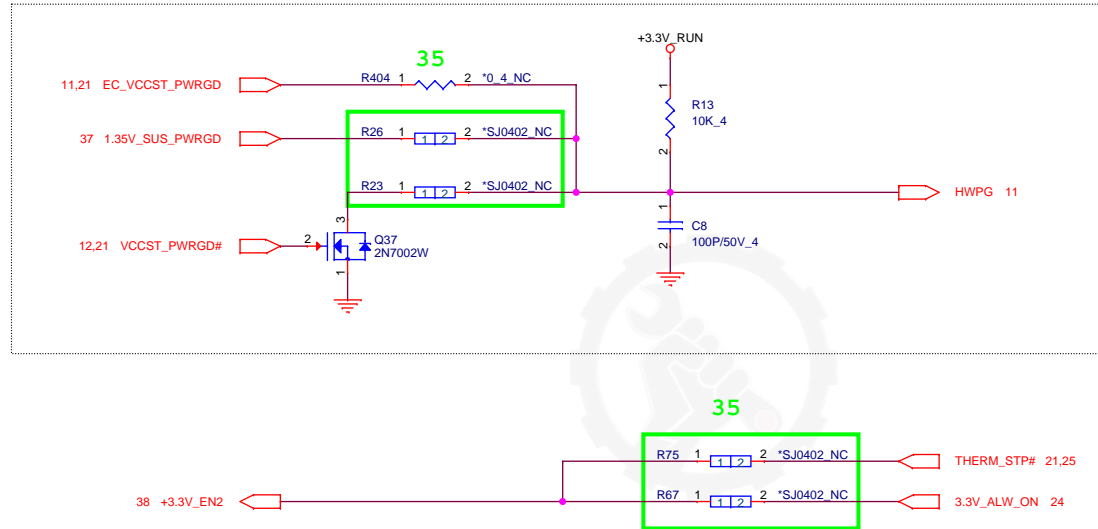
Quanta Computer Inc.
PROJECT : D13C



PROJECT : D13C

Date: Friday, September 27, 2013 Sheet 31 of 44



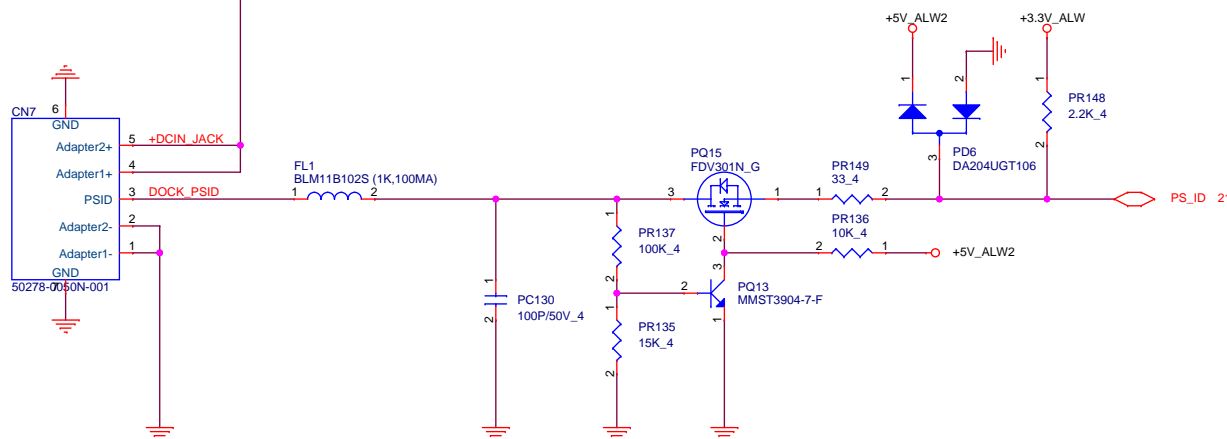
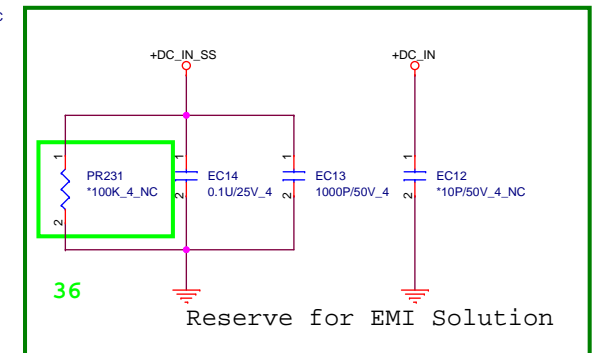
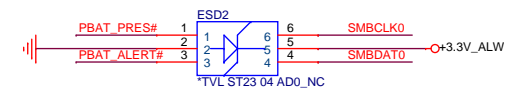
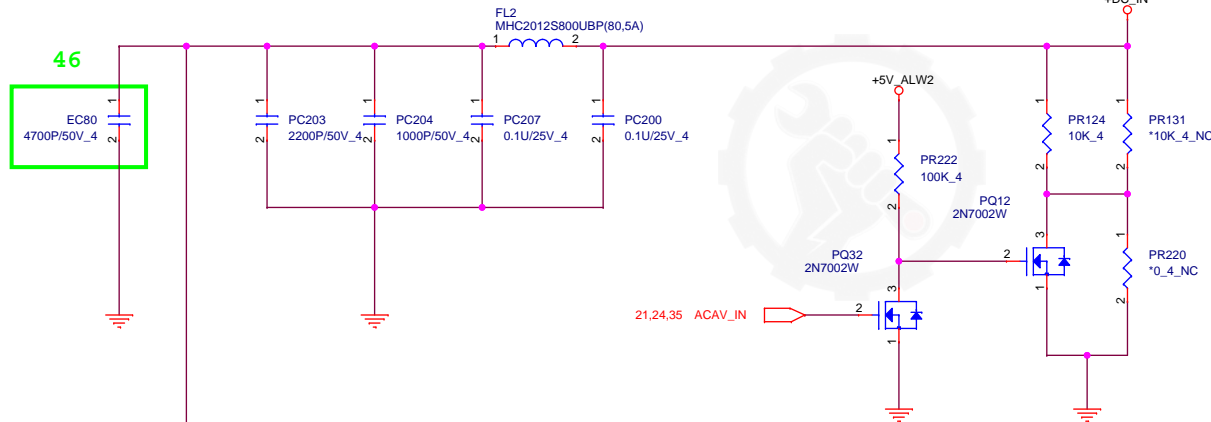
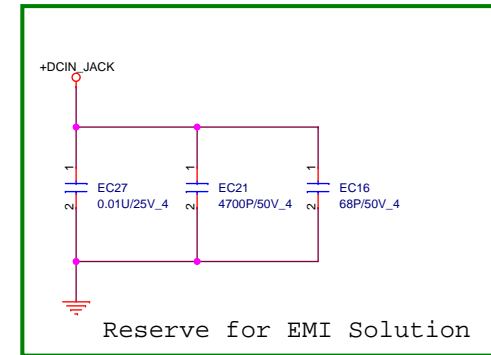
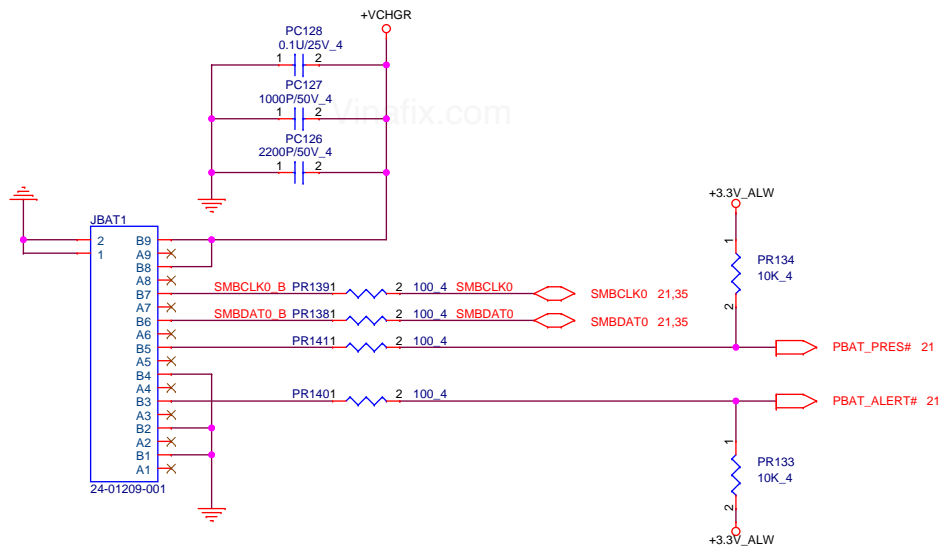


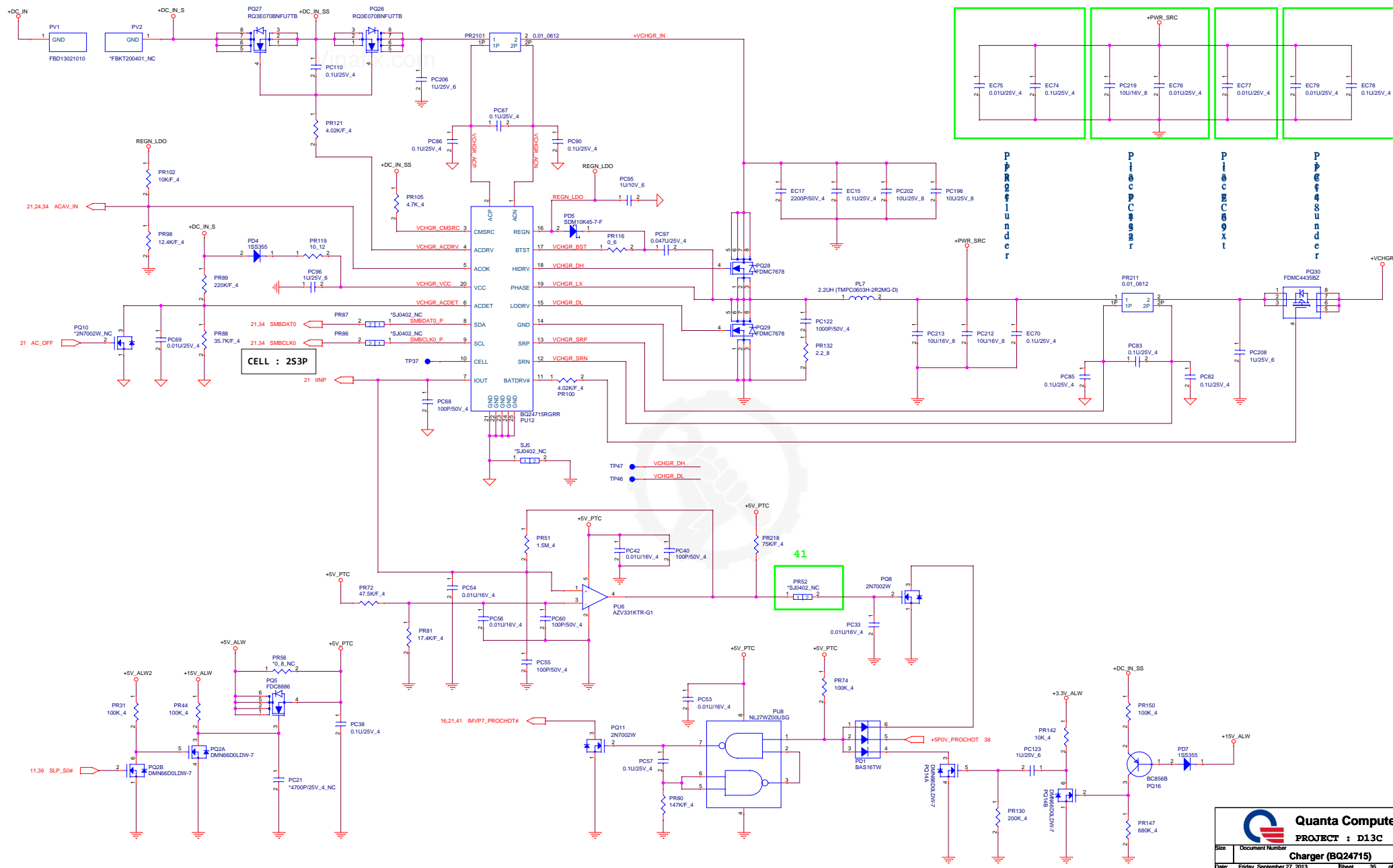
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PROJECT : D13C

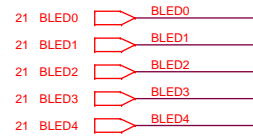
Size	Document Number	Rev
		4A
Date:	Friday, September 27, 2013	Sheet 33 of 44

System Reset Circuit



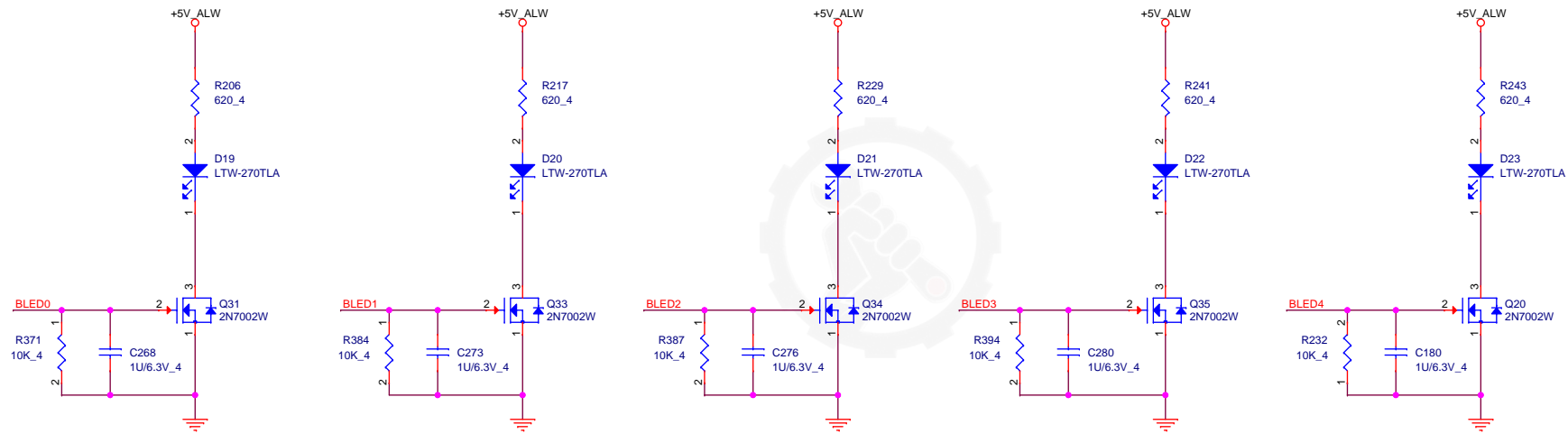


Battery Status LED

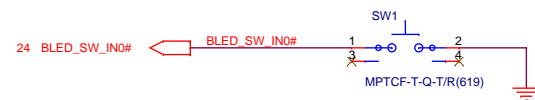


Truth table of Battery LED

Battery Power State	BLED4	BLED3	BLED2	BLED1	BLED0	LED State
<20%	0	0	0	0	0	N/A
20%	0	0	0	0	1	D19
40%	0	0	0	1	1	D19 D20
60%	0	0	1	1	1	D19 D20 D21
80%	0	1	1	1	1	D19 D20 D21 D22
100%	1	1	1	1	1	D19 D20 D21 D22 D23



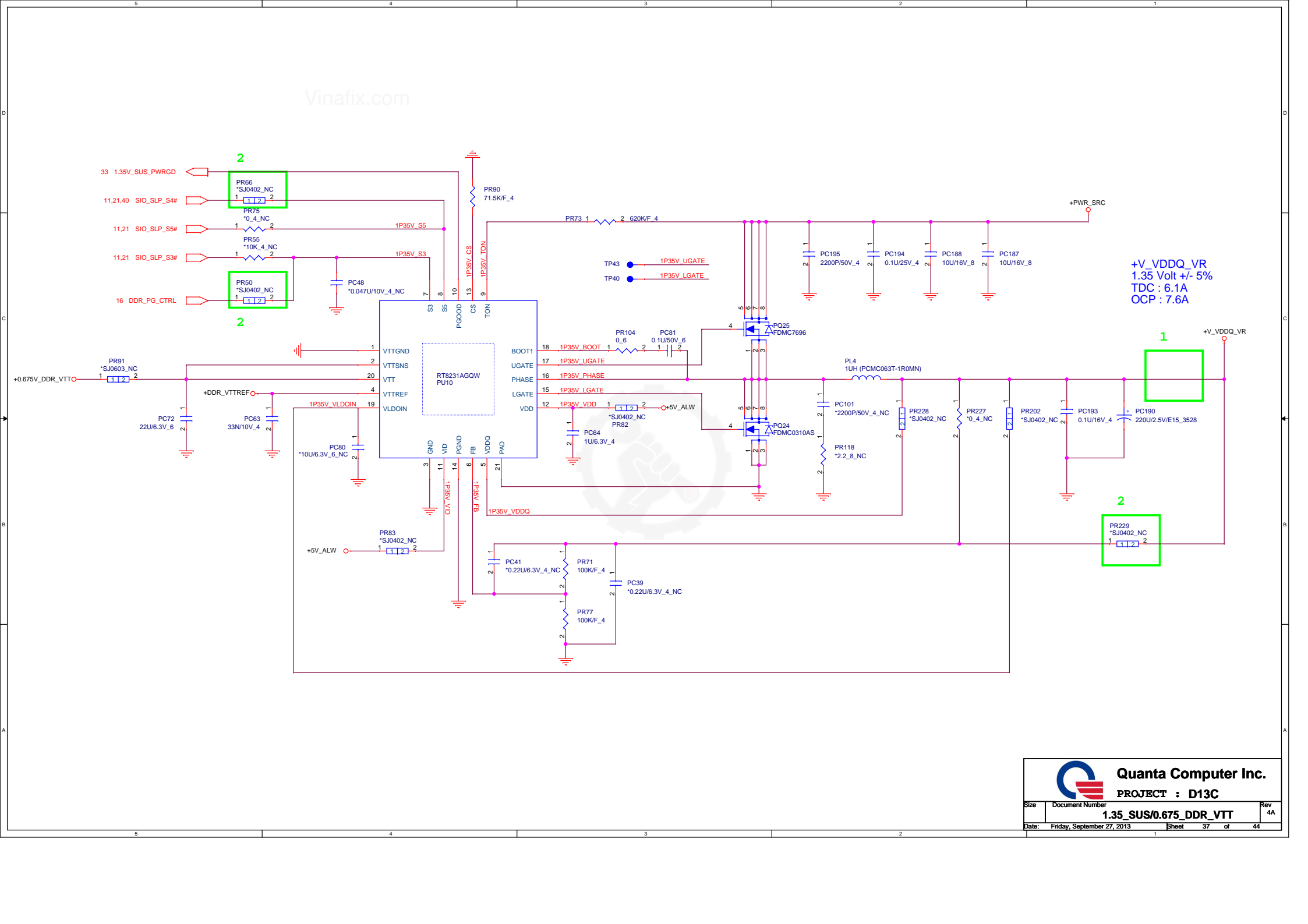
Battery LED button

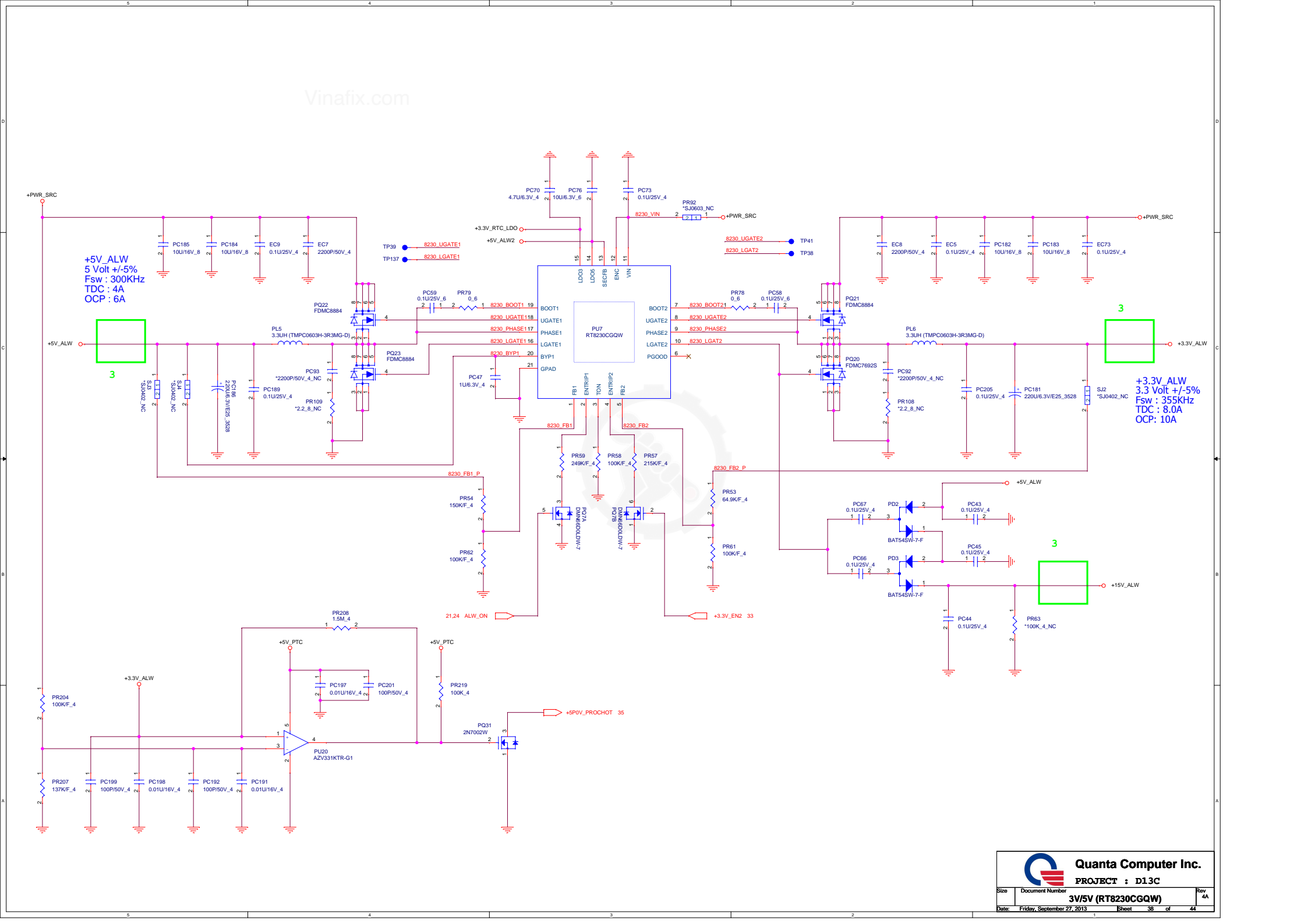


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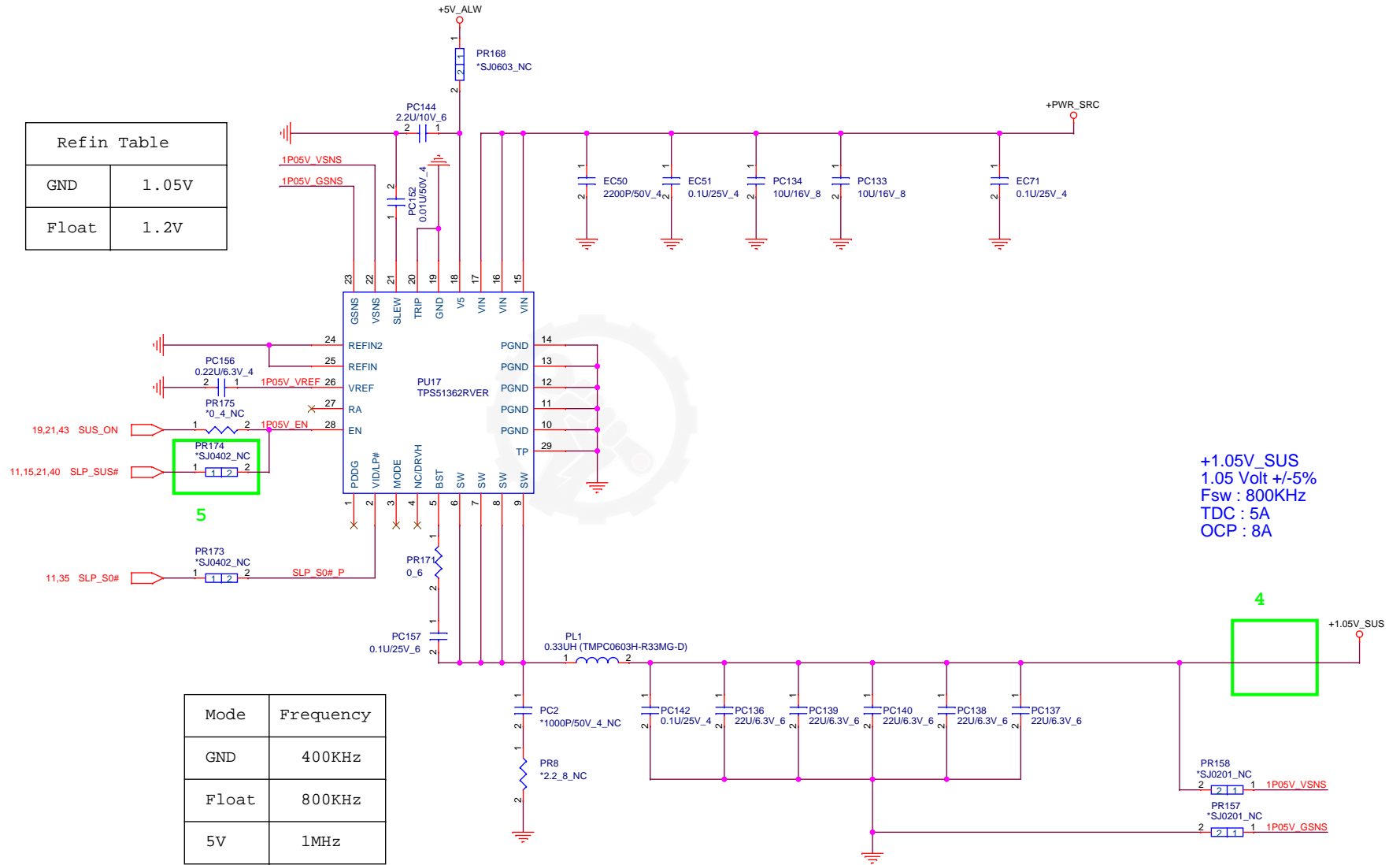
PROJECT : D13C

Size	Document Number	Rev
	LED Switch	4A
Date:	Friday, September 27, 2013	Sheet 36 of 44





Refin Table	
GND	1.05V
Float	1.2V



+1.05V_SUS
1.05 Volt +/-5%
Fsw : 800KHz
TDC : 5A
OCP : 8A

Mode	Frequency
GND	400KHz
Float	800KHz
5V	1MHz



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PROJECT : D13C

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+5V_ALW

PU21
RT8068AZQW

PGOOD LX1 LX2 LX3 NC FB EN

PC217 10U/6.3V_6

EC66 0.1U/25V_4

PC211 1U/6.3V_4

PC209 0.047U/25V_4

PC210 *22P/50V_4_NC

PL8 2.2UH (FDV0530S-H-2R2M=P3)

PC216 0.1U/25V_4

PC214 22U/6.3V_6

PC215 22U/6.3V_6

PR215 102K/F_4

PR214 51.1K/F_4

*0.4_NC PR212

*SJ0402_NC PR213

SIO_SLP_S4# 11,21,37

SLP_SUS# 11,15,21,39

+1.8V_SUS

6

+1.8V_SUS
1.8 Volt +/- 5%
Fsw : 1MHz
TDC : 0.85A
OCP : 3.0A

+1.8V_SUS

PC62 10U/6.3V_6

PR84 10K/F_4

PC71 1U/6.3V_4

PC61 0.047U/25V_4

PC74 10U/6.3V_6

PC75 *10U/6.3V_6_NC

PC79 *0.1U/16V_4_NC

PR101 10K/F_4

PR93 11.5K/F_4

G9661-25ADJ/TP1U PU11

VIN VO

VEN ADJ

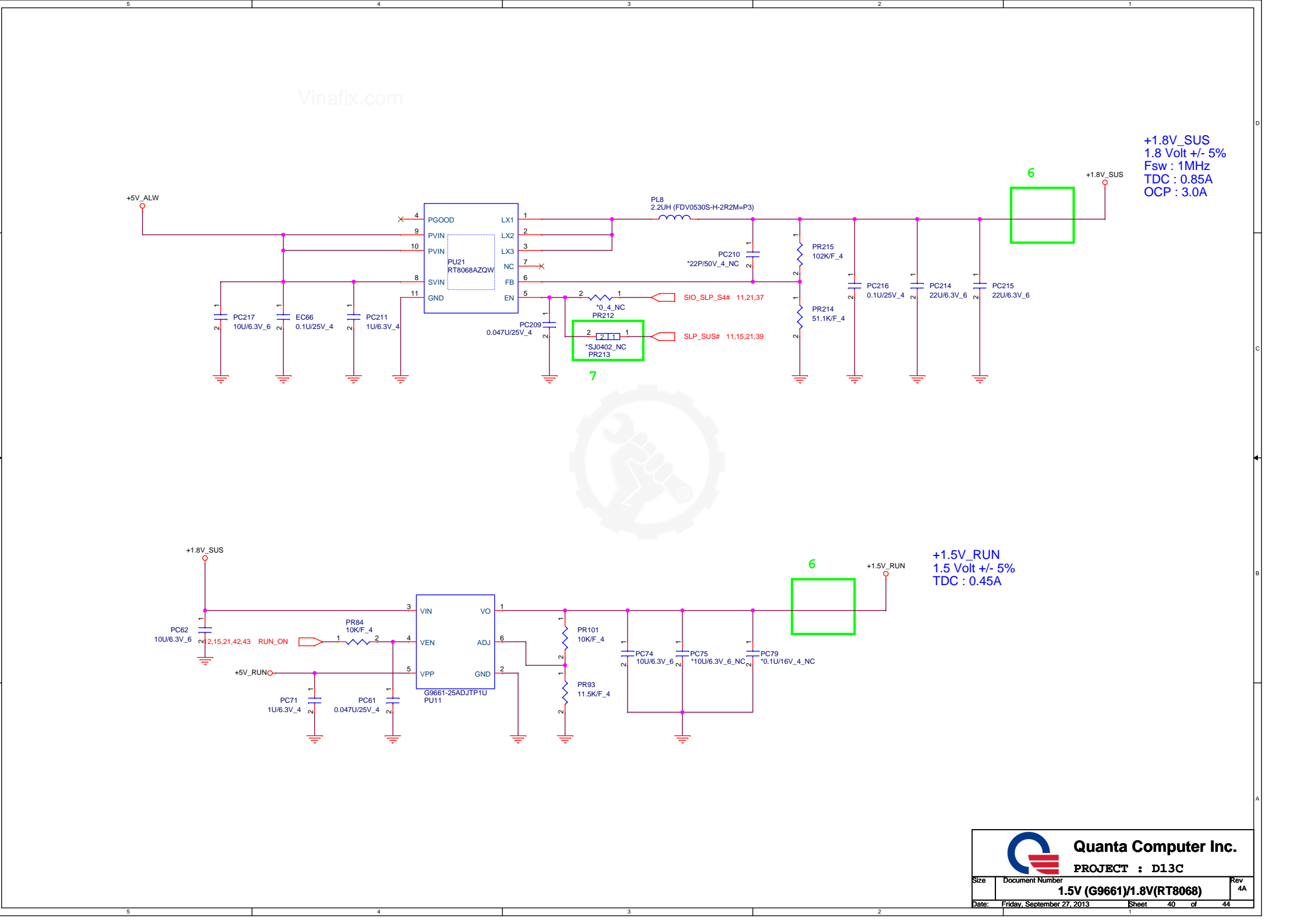
VPP GND

+1.5V_RUN

6

+1.5V_RUN
1.5 Volt +/- 5%
TDC : 0.45A

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PROJECT : D13C
1.5V (G9661)/1.8V(RT8068)
Date: Friday, September 27, 2013 Sheet 40 of 44 Rev 4A



Vinafix.com

+5V_ALW

PU21
RT8068AZQW

PGOOD
PVIN
SVIN
GND

LX1
LX2
LX3
NC
FB
EN

PC217 10U/6.3V_6
EC66 0.1U/25V_4
PC211 1U/6.3V_4
PC209 0.047U/25V_4
PC210 *22P/50V_4_NC
PC216 0.1U/25V_4
PC214 22U/6.3V_6
PC215 22U/6.3V_6
PR215 102K/F_4
PR214 51.1K/F_4
PL8 2.2UH (FDV0530S-H-2R2M=P3)
PR212 *0.4_NC
PR213 *SJ0402_NC
SIO_SLP_S4# 11,21,37
SLP_SUS# 11,15,21,39

+1.8V_SUS
1.8 Volt +/- 5%
Fsw : 1MHz
TDC : 0.85A
OCP : 3.0A

+1.8V_SUS

+1.8V_SUS

+1.5V_RUN
1.5 Volt +/- 5%
TDC : 0.45A

+1.5V_RUN

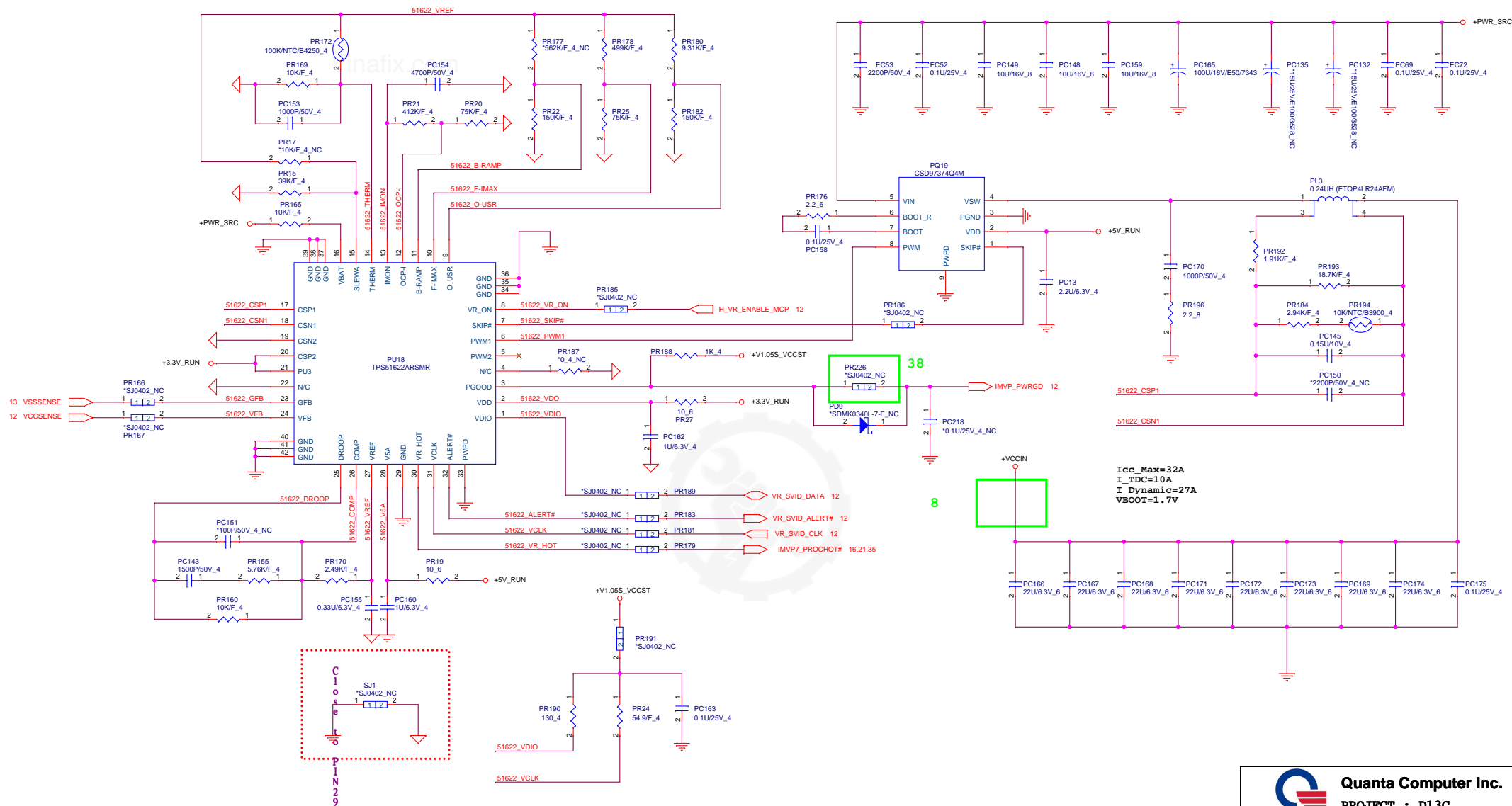
PC62 10U/6.3V_6
PC71 1U/6.3V_4
PC61 0.047U/25V_4
PR84 10K/F_4
PR101 10K/F_4
PR93 11.5K/F_4
PC74 10U/6.3V_6
PC75 *10U/6.3V_6_NC
PC79 *0.1U/16V_4_NC
G9661-25ADJ/TP1U
PU11

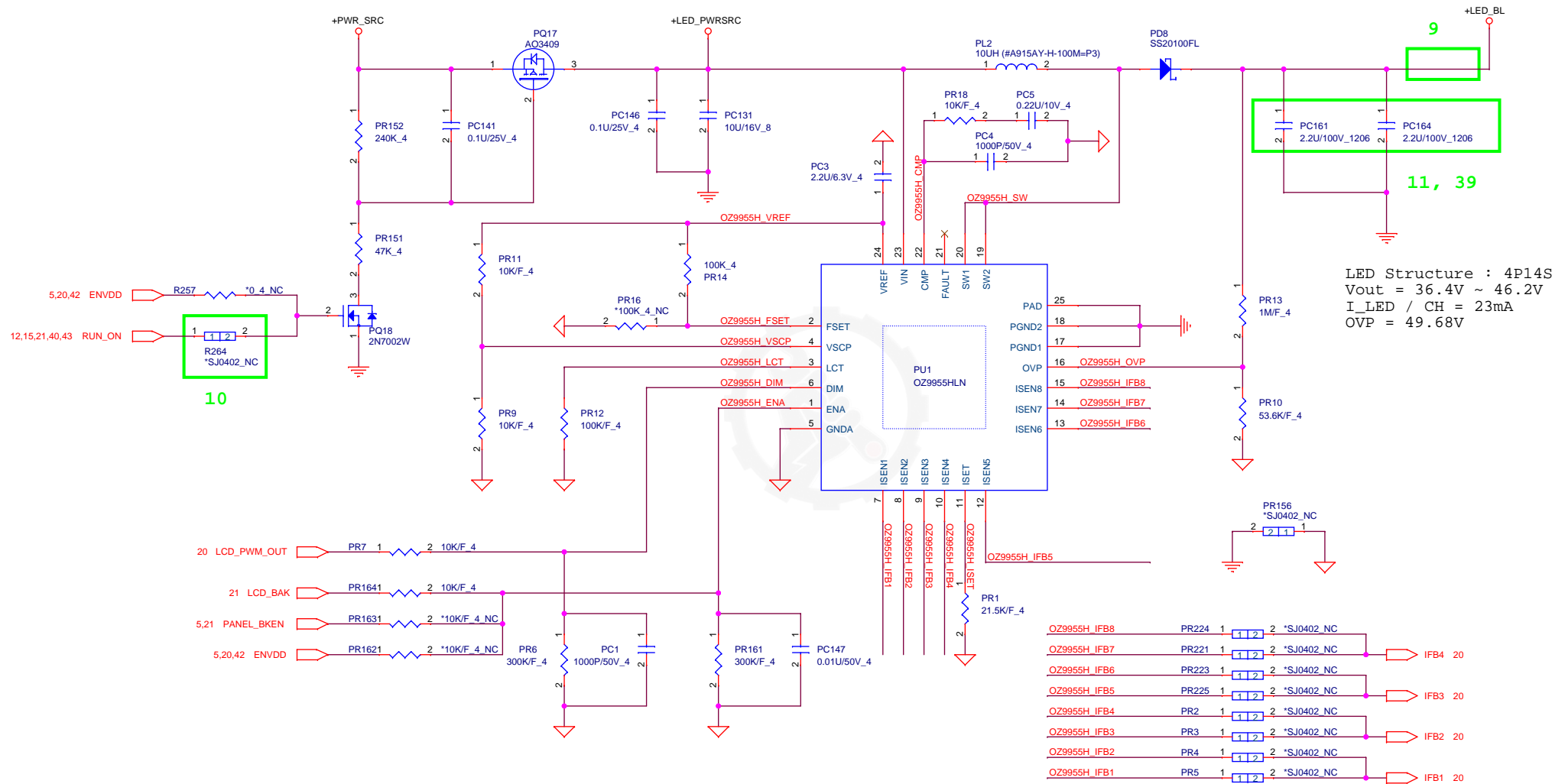
VIN
VEN
VPP
GND

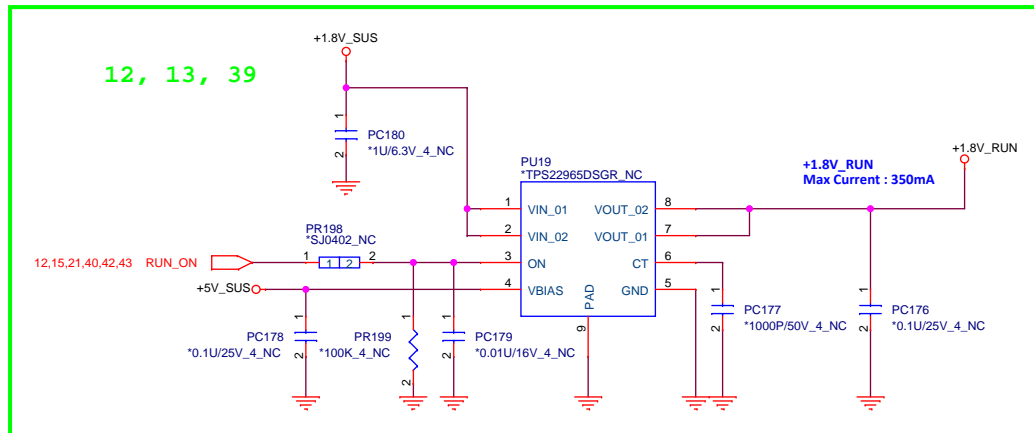
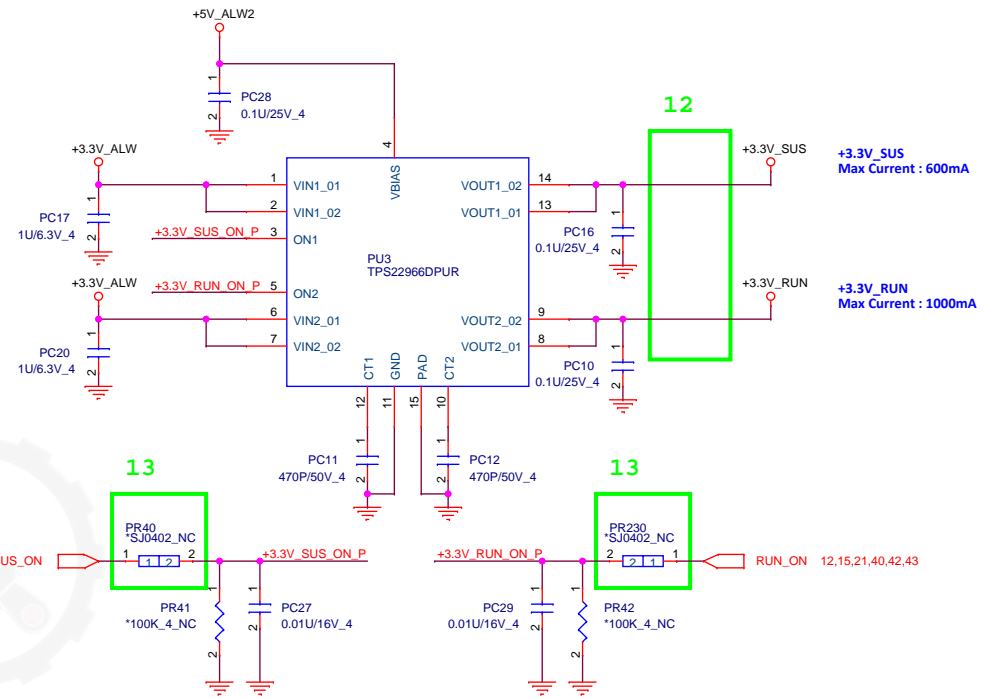
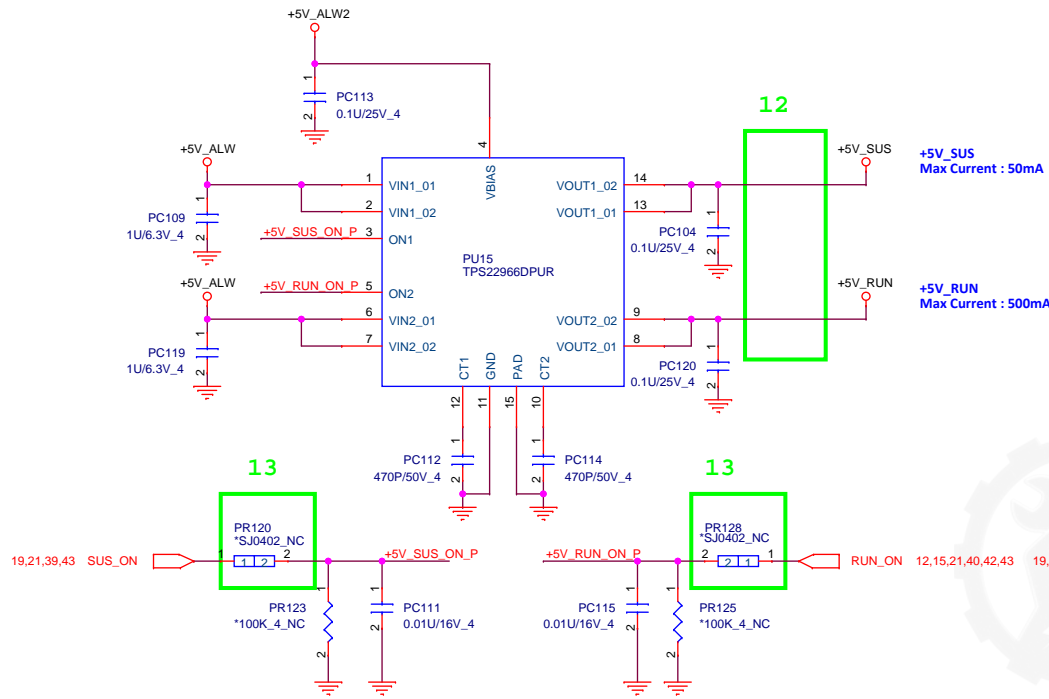
VO
ADJ
GND

1.5V (G9661)/1.8V(RT8068)

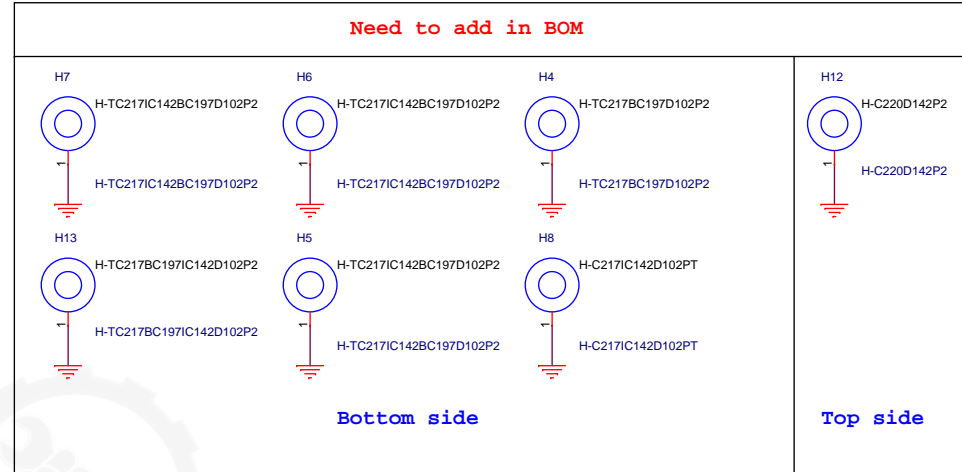
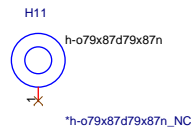
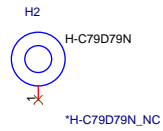
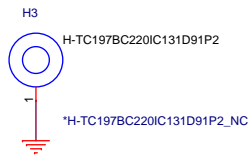
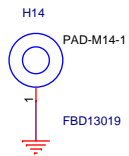
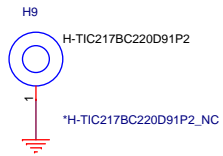
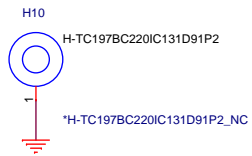
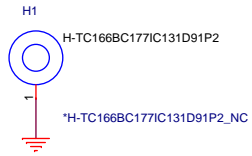
Quanta Computer Inc.
PROJECT : D13C
1.5V (G9661)/1.8V(RT8068)
Date: Friday, September 27, 2013
Sheet 40 of 44
Rev 4A







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PROJECT : D13C



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PROJECT : D13C